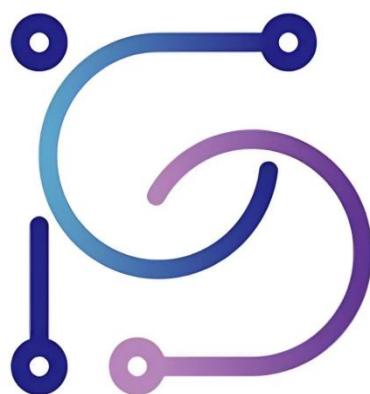




INDIESEMIC

ISC-nRF54L15-A

An advanced multi-protocol ultra-low power BLE Module

DATASHEET

Version: V2.2

Revision history:

Revision	Description	Date
1.0	– Initial Release	20/08/2025
2.0	– Restructured datasheet – Added FAQ – Power Consumption data – Reflow Diagram	27/05/2026
2.1	– Applied Copyright – Certified for FCC/C and WPC – Updated pin-out and Connection table	26/06/2026
2.2	– Added Shield Image	28/07/2026

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1. Description

ISC-nRF54L15-A is an Integrated multi-purpose MCU functionality which supports Nordic's nRF54L Series SoCs which is suited to enable a broad range of applications. The multiprotocol 2.4 GHz radio supports the latest Bluetooth® 6.0 features including Bluetooth Channel Sounding, as well as 802.15.4-2020 for standards such as Thread, Matter, and Zigbee, and a proprietary 2.4 GHz mode supporting up to 4 Mbps for higher throughput. The module integrates the peripherals expected in a wireless microcontroller enabling many products to be implemented with a single chip. An integrated RISC-V coprocessor further reduces the need for external ICs.

This module comes with lower power consumption, ISC-nRF54L15-A module enables improved battery lifetime and reduced battery size including pin-to-pin compatible options with several memory options.

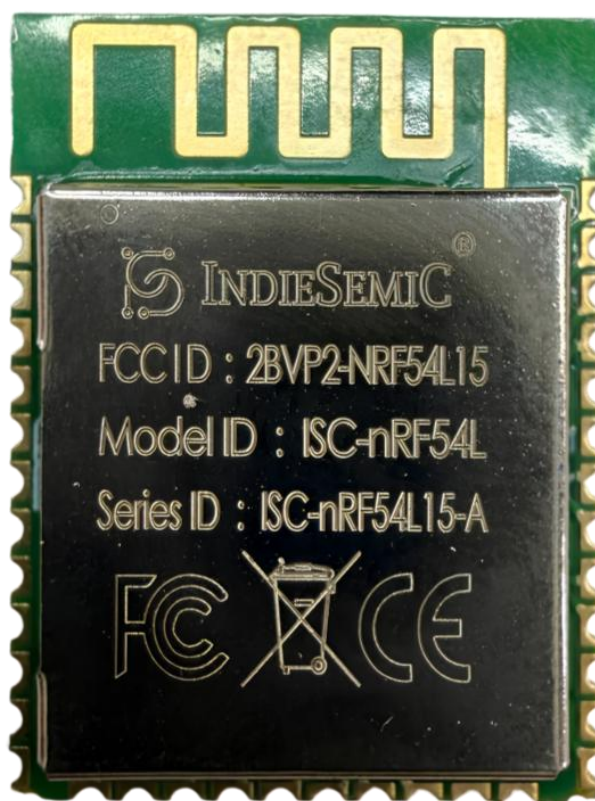


Figure 1- ISC-nRF54L15-A

2. Features

- ▶ Bluetooth® 6.0, IEEE 802.15.4-2020, 2.4 GHz transceiver
 - -96 dBm sensitivity in 1 Mbps Bluetooth® Low Energy mode, 0.1% bit error rate
 - +8 dBm TX power (down to -8 dBm)
 - RSSI (1 dB resolution)
- ▶ Supported data rates:
 - Bluetooth® 6.0 – 2 Mbps, 1 Mbps, 500 kbps, and 125 kbps
 - Proprietary 2.4 GHz – 4 Mbps, 2 Mbps, 1 Mbps
- ▶ Arm® Cortex®-M33 TrustZone® technology 32-bit processor with FPU, 128 MHz
 - 500 EEMBC CoreMark® score running from flash memory
 - 3.90 CoreMark/MHz
 - Watchpoint and trace debug modules (DWT, ETM, and ITM)
 - Serial Wire Debug (SWD) support
- ▶ 1500 kB RRAM (non-volatile memory) and 256 kB RAM
- ▶ Advanced on-chip features
 - NFC-A tag with wake-on-field capability
 - Programmable Peripheral Interconnect (PPI)
 - 29 General Purpose I/O (GPIO) pins
 - EasyDMA automated data transfer between memory and peripherals
- ▶ 128-bit AES/ECB/CCM/AAR cryptographic coprocessor
- ▶ On-the-fly packet encryption support
- ▶ ADC support
 - 14-bit at 31.25 ksps
 - 12-bit at 250 ksps
 - 10-bit at 2 Msps
- ▶ 8 configurable ADC channels with programmable gain
- ▶ Three pulse width modulator (PWM) units with EasyDMA
- ▶ Seven 32-bit timers with counter mode
- ▶ Up to five fully featured serial interfaces with EasyDMA, supporting I2 C, SPI controller/peripheral, and UART
 - One high-speed SPIM up to 32 MHz, four up to 8 MHz
 - One high-speed UARTE up to 4 Mbps, four up to 1 Mbps
 - I2 C up to 400 kHz
- ▶ I2S two-channel inter-IC sound interface
- ▶ UART with CTS/RTS and EasyDMA
- ▶ Quadrature Decoder (QDEC)
- ▶ Real-Time Counters (RTC)
- ▶ Integrated temperature sensor
- ▶ Global RTC (GRTC) that can run in System OFF mode and implement a shared system timer
- ▶ Pulse density modulation (PDM) interface
- ▶ Near field communication (NFC)
- ▶ Up to two quadrature decoders (QDEC)
- ▶ Comparator and low-power comparator with wake-up from System OFF mode

3. Applications

- ▶ Advanced computer peripherals and I/O devices
 - Mouse
 - Keyboard
 - Multi-touch trackpad
- ▶ Internet of things (IOT)
 - Smart home products
 - Industrial mesh networks
 - Smart city infrastructure
- ▶ Advanced wearable devices
 - Connected watches
 - Advanced personal fitness devices
 - Wearables with wireless payment
 - Connected health devices
 - Virtual/Augmented Reality (VR/AR) applications
- ▶ Interactive entertainment devices
 - Advanced remote controls
 - Gaming controllers
- ▶ Personal area networks
 - Health/Fitness sensor and monitoring devices
 - Medical devices
 - Smart home products
 - Industrial mesh networks
 - Smart city infrastructure

4. Block Diagram

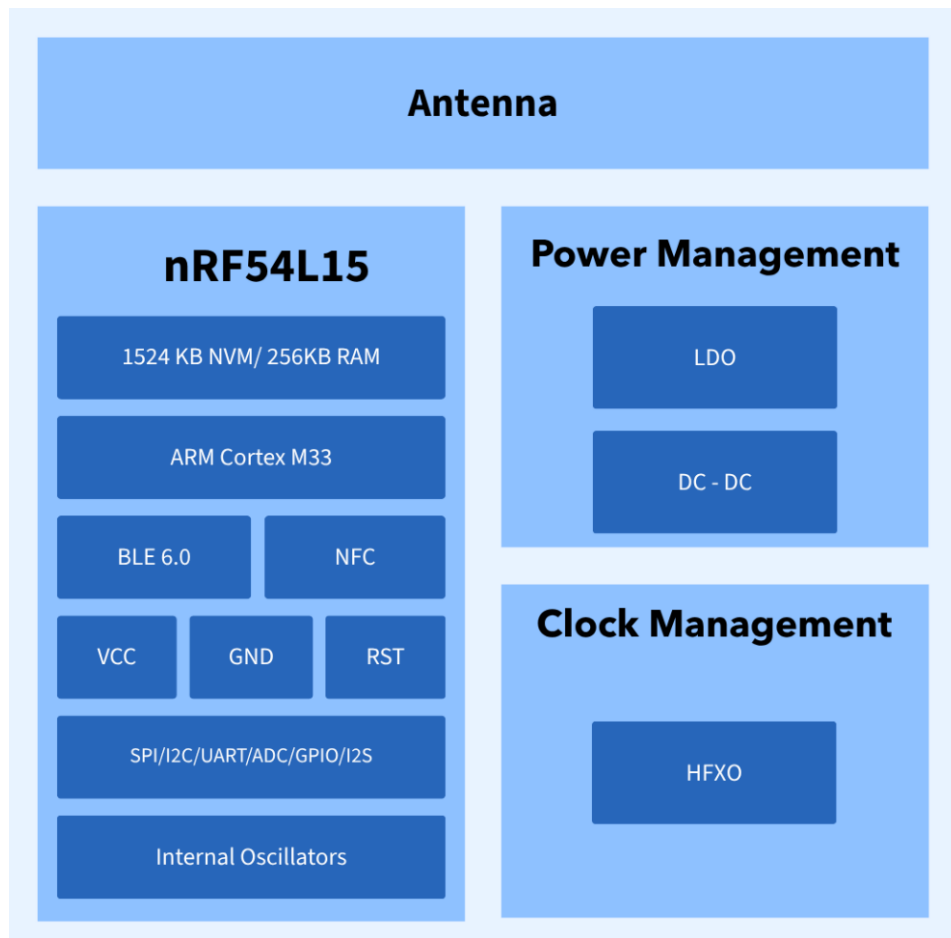


Figure 2- Block Diagram

5. Module Pin-out

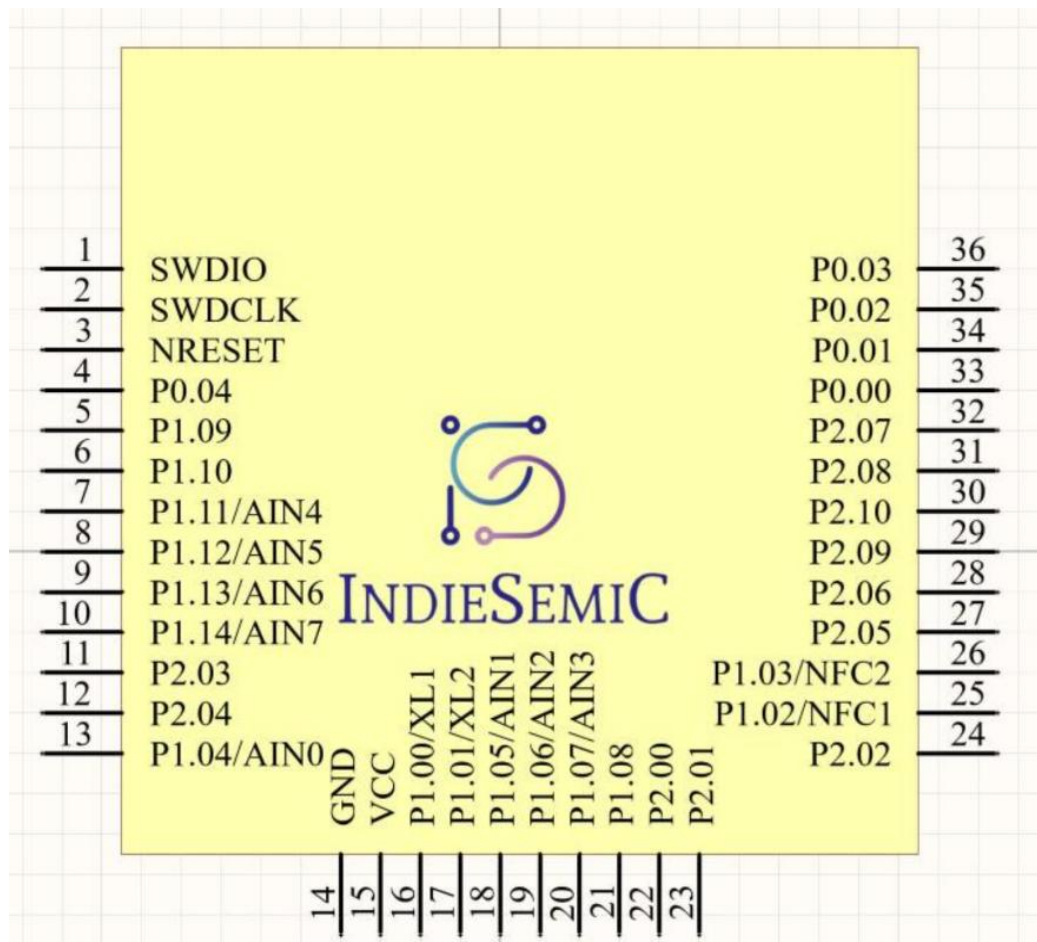


Figure 3- Module Pinout (front view)

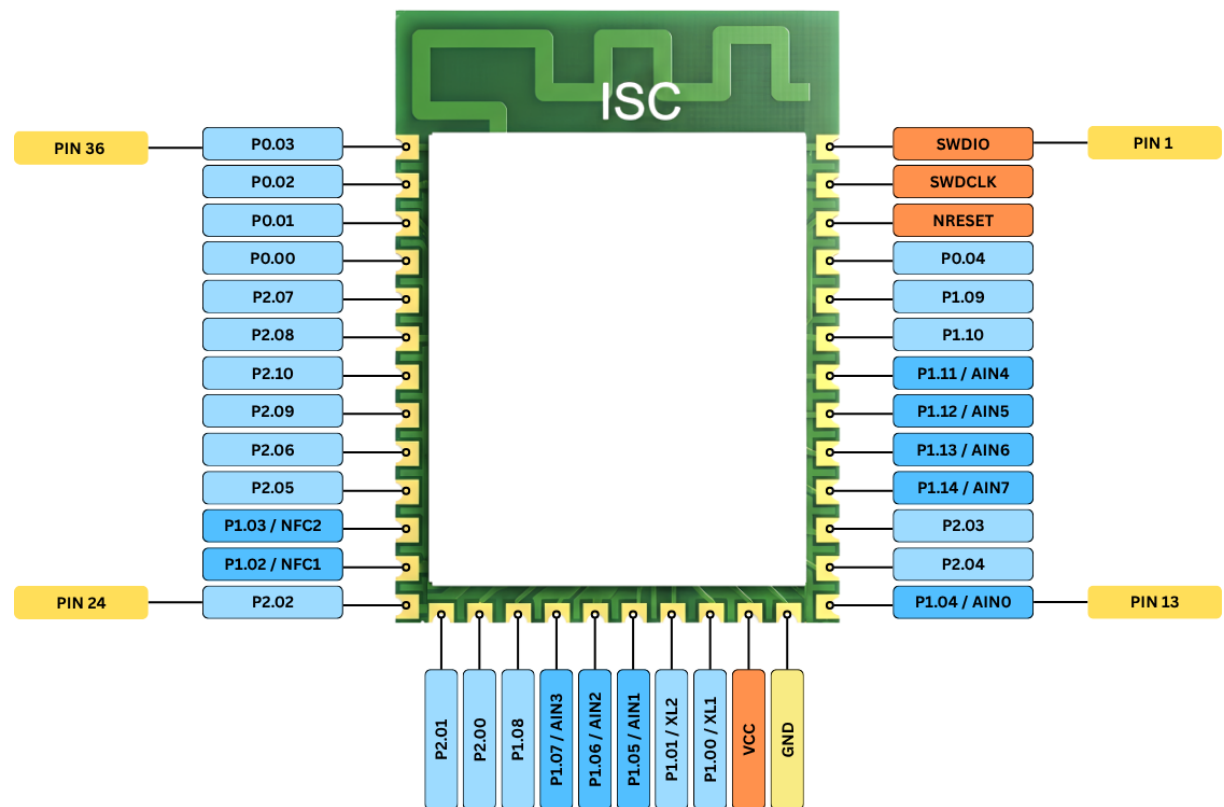


Figure 4 - Pin Diagram (Back View)

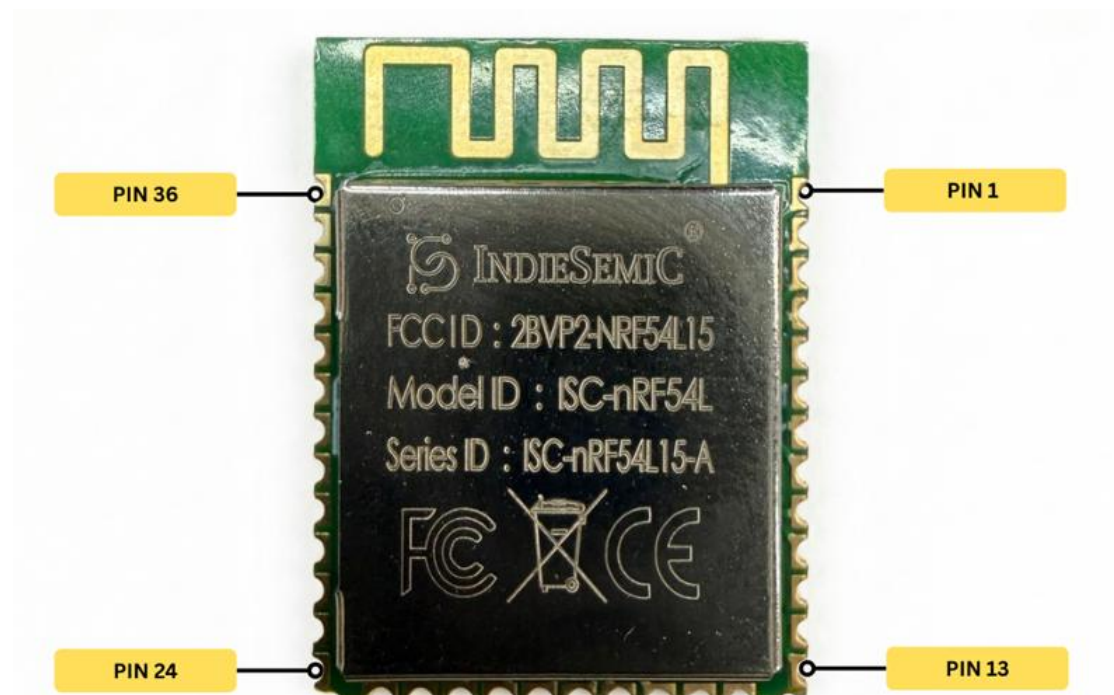


Figure 5 - Pin Diagram (front view)

6. PCB Footprint

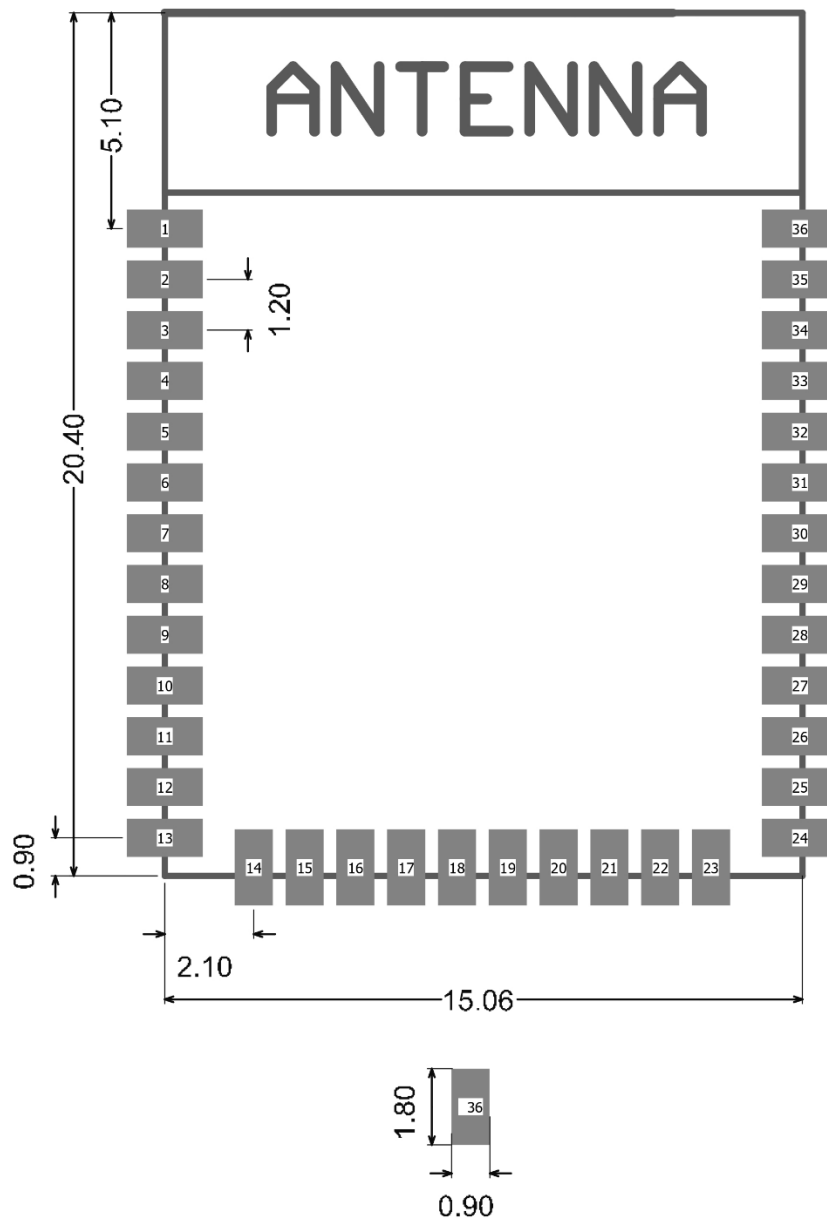


Figure 6 - PCB Footprint (front)

7. Pin Descriptions

Pin No.	Name	I/O Type	Description
1	SWDIO	Digital I/O	Programming Clock
2	SWDCLK	Digital Input	Digital Data
3	NRESET	RESET	Reset Pin
4	P0.04	Digital I/O	General-Purpose I/O
5	P1.09	Digital I/O	General-Purpose I/O
6	P1.10	Digital I/O	General-Purpose I/O
7	P1.11	Digital I/O	General-Purpose I/O
8	P1.12	Digital I/O	General-Purpose I/O
9	P1.13	Digital I/O	General-Purpose I/O
10	P1.14	Digital I/O	General-Purpose I/O
11	P2.03	Digital I/O	General-Purpose I/O
12	P2.04	Digital I/O	General-Purpose I/O
13	P1.04/AIN0	Digital I/O / AIN0	General-Purpose I/O / Analog Input
14	GND	Ground	Ground
15	VCC	Power	Power Supply
16	P1.00/XL1	Digital I/O / LFXO	General-Purpose I/O / LFXO
17	P1.01/XL2	Digital I/O / LFXO	General-Purpose I/O / LFXO
18	P1.05/AIN1	Digital I/O / AIN1	General-Purpose I/O / Analog Input
19	P1.06/AIN2	Digital I/O / AIN2	General-Purpose I/O / Analog Input
20	P1.07/AIN3	Digital I/O / AIN3	General-Purpose I/O / Analog Input
21	P1.08	Digital I/O	General-Purpose I/O
22	P2.00	Digital I/O	General-Purpose I/O
23	P2.01	Digital I/O	General-Purpose I/O
24	P2.02	Digital I/O	General-Purpose I/O
25	P1.02/NFC1	Digital I/O	General-Purpose I/O
26	P1.03/NFC2	Digital I/O	General-Purpose I/O
27	P2.05	Digital I/O	General-Purpose I/O
28	P2.06	Digital I/O	General-Purpose I/O
29	P2.09	Digital I/O	General-Purpose I/O

30	P2.10	Digital I/O	General-Purpose I/O
31	P2.08	Digital I/O	General-Purpose I/O
32	P2.07	Digital I/O	General-Purpose I/O
33	P0.00	Digital I/O	General-Purpose I/O
34	P0.01	Digital I/O	General-Purpose I/O
35	P0.02	Digital I/O	General-Purpose I/O
36	P0.03	Digital I/O	General-Purpose I/O

Table 1- Pin Descriptions

**Before selecting any GPIO please refer [here](#) to check the functionality of the pins .*

8. Electrical Specifications

8.1 Absolute Maximum Ratings

Parameter	Condition	Min.	Typical	Max.
Storage Temperature		-40		105 °C
ESD Protection	HBM			1000 V
Supply Voltage	VDD-NRF	-0.3 V		3.6 V
Voltage on Any I/O Pin	VI/O, VDD ≤ 3.5 V	-0.3 V		VDD+0.3
	VI/O, VDD > 3.5 V	-0.3 V		3.6 V

Table 2- Maximum Rating

8.2 Recommended Operating Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temperature	TA	-40	25	85	°C
Power Supply	VCC	1.7	3.3	3.5	V
Input Low Voltage	VIL	0		0.3×VCC	V
Input High Voltage	VIH	0.7×VCC		VCC	V

Table 3- Operating Ratings

9. Function Description

9.1.1 GPIO Ports and Pin Planning Summary

The nRF54L15 organizes its General-Purpose Input/Output (GPIO) pins into three independent ports, each mapped to a specific power domain to optimize performance, power efficiency, and functional flexibility. The available ports are P2 (MCU domain), P1 (Peripheral domain), and P0 (Low-power domain). The RADIO domain does not include GPIO pins.

Each GPIO port supports configurable pin direction, internal pull-up and pull-down resistors, and programmable drive strength, allowing flexible signal interfacing and optimized power usage.

9.1.2 GPIO Port 2 (P2): MCU Domain (High-Speed Interface Port)

- ▶ Designed for high-speed digital signals and performance-critical interfaces
- ▶ Supports signal speeds up to 64 MHz
- ▶ Available drive modes: standard, high drive, and extra high drive
- ▶ Used by high-speed peripherals such as SPIM00 and UARTE00
- ▶ Dedicated pins for TRACE interface and RISC-V FLPR co-processor peripherals (Soft Peripherals)
- ▶ Does not support GPIO interrupts, pin sense, or wake-up from sleep
- ▶ Best suited for fast serial communication and debugging interfaces

9.1.3 GPIO Port 1 (P1): Peripheral Domain (Main I/O Port)

- ▶ General-purpose port optimized for application peripherals
- ▶ Supports signal speeds up to 8 MHz
- ▶ Available drive modes: standard and high drive
- ▶ Supports wake-up from System ON and System OFF low-power modes
- ▶ Includes analog-capable pins (AIN0–AIN7) shared with ADC and comparator peripherals
- ▶ Exclusive support for PWM outputs
- ▶ Supports pin sense mechanism and GPIOTE interrupt events
- ▶ Provides dedicated pins for:
 - NFC antenna interface
 - Low-frequency crystal oscillator (32.768 kHz LFXO)
 - Tamper detection interface (TAMPC)
 - Bluetooth direction-finding radio signals

9.1.4 GPIO Port 0 (P0): Low-Power Domain (Always-On I/O Port)

- ▶ Optimized for ultra-low-power operation
- ▶ Supports signal speeds up to 8 MHz
- ▶ Available drive modes: standard and high drive
- ▶ Supports wake-up from System ON and System OFF modes
- ▶ Supports pin sense mechanism and GPIOTE interrupt events

- Includes dedicated support for Global RTC (GRTC) clock and PWM output functions
- Ideal for always-on sensors and low-power wake-up sources

9.1.5 Two Wire Interface

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching and supporting data rates of 100 kbps, 250kbps 400kbps and 1000 kbps.

9.1.6 Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

9.1.7 Serial Peripheral Interface

The nRF54L15 provides multiple high-performance SPI Master (SPIM) and SPI Slave (SPIS) interfaces supporting full-duplex synchronous communication over standard 4-wire SPI (SCK, MOSI, MISO, CSN). The SPI peripherals support SPI modes 0, 1, 2, and 3 and include EasyDMA for efficient data transfer between RAM and peripheral hardware with minimal CPU load.

SPI signals are routed through programmable pin selection, allowing flexible GPIO assignment and optimized PCB routing. Chip select signals are controlled by the application using GPIOs, enabling multi-slave bus configurations.

▸ SPI Instance Overview

SPI Master (SPIM) Instances

- SPIM00
- SPIM20
- SPIM21
- SPIM22

SPI Slave (SPIS) Instances

- SPIS00 — Dedicated high-speed pins on P2
- SPIS20 — P1 or dedicated P2 pins
- SPIS21 — P1 or dedicated P2 pins
- SPIS22 — P1 pins
- SPIS30 — P0 pins

***Note:**

Some SPI instances share internal hardware resources with TWIM/TWIS (I²C) and UARTE peripherals when mapped to the same peripheral ID. Only one peripheral per shared ID group can be enabled at a time. Designers must verify the nRF54L15 instantiation table when selecting SPI instances to avoid resource conflicts. And their properties are as below:

Instance	Master/Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

Table 4 - SPI

***Note:** You can also refer to [nrf54L pin planner](#) to check peripheral supported by all the pins.

9.1.8 UART's

The nRF54L15 provides multiple UARTE (UART with EasyDMA) interfaces supporting high-speed, full-duplex, asynchronous serial communication. The UARTE peripherals include hardware flow control (CTS/RTS) and parity checking, enabling reliable data transfer with minimal CPU intervention.

All UARTE instances support separate EasyDMA engines for TX and RX, allowing data transfers directly between RAM and peripheral hardware while the CPU remains idle or in low-power states.

Baud UARTE Instance Overview

The nRF54L15 includes the following UART instances:

- UARTE00 — High-speed UART (up to 4 Mbps), uses dedicated P2 (MCU domain) pins
- UARTE20 — Peripheral domain UART, uses P1 or selected dedicated P2 pins
- UARTE21 — Peripheral domain UART, uses P1 or selected dedicated P2 pins
- UARTE22 — Peripheral domain UART, uses P1 or selected dedicated P2 pins
- UARTE30 — Low-power UART, uses P0 (LP domain) pins only

GPIO Routing Notes

- UART pins (TXD, RXD, CTS, RTS) are assigned through programmable pin selection registers
- GPIO routing is constrained by power domain and dedicated pin rules

- ▶ Pins from different GPIO ports cannot be mixed within the same UART instance
- ▶ Only approved dedicated P2 pins may be used for cross-domain routing

9.1.9 Analogue to Digital Converter

The nRF54L15 integrates a high-performance Successive Approximation (SAR) ADC (SAADC) that enables accurate sampling of multiple analog signals for sensor interfacing, battery monitoring, and analog measurement applications.

The SAADC supports up to 8 analog input channels (AIN0–AIN7) selectable through an internal multiplexer. Each channel can be configured for single-ended or differential input operation.

ADC Features:

- ▶ Differential SAR ADC architecture
- ▶ Up to 8 multiplexed analog input channels
- ▶ Configurable resolution and performance modes:
 - 10-bit mode up to 2 MS/s
 - 12-bit mode up to 250 kS/s
 - 14-bit mode (with oversampling) up to 31.25 kS/s
- ▶ Hardware-supported oversampling and averaging
- ▶ Programmable input scaling and reference selection
- ▶ EasyDMA support for efficient RAM data transfer

Shared Analog Resource Note

- The SAADC shares analog input resources with the Low-Power Comparator (LPCOMP) module.
- SAADC and LPCOMP can operate simultaneously,
- But the same analog input pin (AINx) must not be selected by both peripherals at the same time.
- Proper channel allocation is required to avoid functional conflicts.

Analog Input Pin Availability

Module PIN Number	ISC-nRF54L15-A PIN Number	Description
13	P1.04/AIN0	Analog-to-Digital Converter
18	P1.05/AIN1	Analog-to-Digital Converter
19	P1.06/AIN2	Analog-to-Digital Converter
20	P1.07/AIN3	Analog-to-Digital Converter

Table 5 - ADC

Design Guidelines

- Avoid assigning the same AIN pin to both SAADC and LPCOMP
- Use oversampling modes for higher resolution and improved noise performance
- Select appropriate sampling speed based on power and accuracy requirements
- Verify analog-capable pins during PCB layout planning

9.1.10 Reset

The reset pin of the module is in the internal pull-high state. When the reset pin of the module is input to a low level, the module will be automatically reset.

After the reset pin is used, the parameters of the current setting will not be ANT.

9.1.11 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analogue inputs on the device. Additionally, the low power comparator can be used as an analogue wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

9.1.12 NFC

The NFC peripheral (referred to as the 'NFC' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum.

With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

- ▶ NFC-A listen mode operation
- ▶ 13.56 MHz input frequency
- ▶ Bit rate 106 kbps
- ▶ Wake-on-field low power field detection (SENSE) mode
- ▶ Frames assemble and disassemble for the NFC-A frames specified by the NFC Forum
- ▶ Programmable frame timing controller

Please Refer [here](#) for More Information related to protocol.

10. Radio Peripherals

The ISC-nRF54L15-A integrates a highly flexible 2.4 GHz multiprotocol transceiver based on Nordic Semiconductor's nRF54L15-A SoC. The device supports Bluetooth® Low Energy (BLE), Bluetooth 6.0, Bluetooth Mesh, IEEE 802.15.4-based protocols including Thread and Zigbee, as well as proprietary 2.4 GHz protocols.

The integrated RF front-end provides a single-ended 50 Ω antenna interface for direct connection to the module antenna. The radio supports programmable transmit power up to +8 dBm and receiver sensitivity down to -103 dBm in Bluetooth LE coded PHY mode, enabling reliable wireless communication with low power consumption.

10.1 Bluetooth Low Energy:

The ISC-nRF54L15-A integrates full Bluetooth Low Energy (BLE) 6.x capability, enabling both high-throughput and long-range operation. Please Refer [Nordic Doc's](#) for More Information related to protocol.

10.2 Bluetooth Mesh:

The ISC-nRF54L15-A fully supports Bluetooth Mesh networking on top of Bluetooth Low Energy. Please Refer [here](#) for More Information related to protocol.

10.3 Thread:

The ISC-nRF54L15-A supports Thread networking based on the IEEE 802.15.4 standard at 2.4 GHz. Please Refer [here](#) for More Information related to protocol.

10.4 Matter:

The ISC-nRF54L15-A is fully capable of running Matter, the unified smart home connectivity standard built on top of IPv6 and Thread. Please Refer [here](#) for More Information related to protocol.

10.5 Zigbee

The ISC-nRF54L15-A supports Zigbee networking using its IEEE 802.15.4 radio. Please Refer [here](#) for More Information related to protocol.

11. Power Consumption Analysis:

The ISC-nRF54L15-A module is designed for ultra-low-power wireless applications with highly optimized BLE performance and efficient system power management. Actual current consumption depends on firmware implementation, radio operating states, peripheral activity, and duty cycle conditions. The power profiles below represent measured values observed during BLE transmission and low-power idle operation.

11.1 System OFF Profile

In System OFF mode, below are the statistics for ISC-nRF54L15-A:

Observed Characteristics:

- ▶ Peak Current: $\sim 10.52 \mu\text{A}$
- ▶ Average Current: $\sim 1.19 \mu\text{A}$
- ▶ Charge Consumption (10 s window): $\sim 11.8 \mu\text{C}$

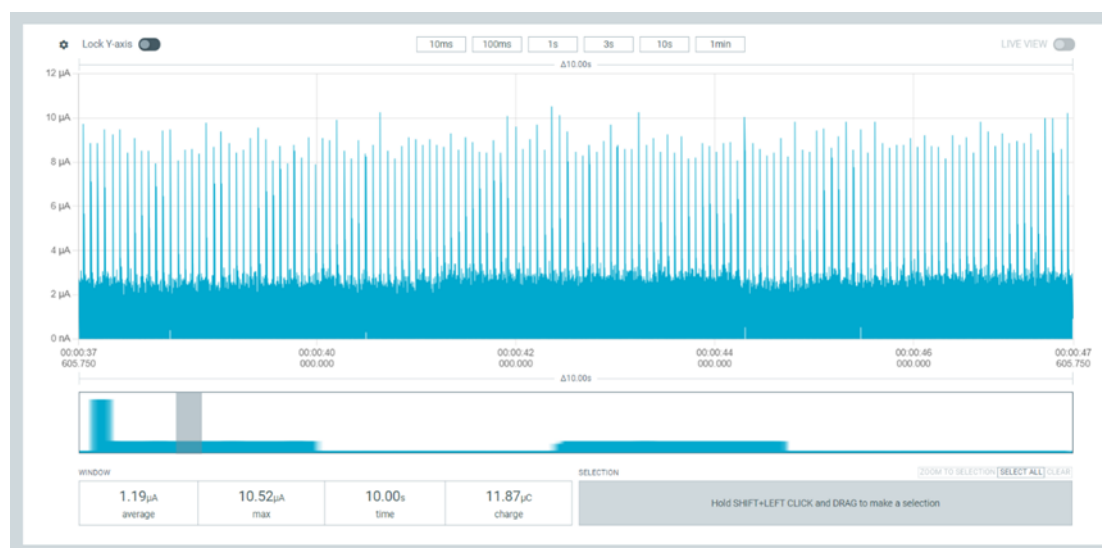


Figure 7 - Low power / ideal current profile

11.2 BLE Advertising Current Profile

During BLE advertising, the module exhibits periodic current spikes corresponding to radio transmission events.

Observed Characteristics:

- ▶ Peak Current @4dBm: ~9.3 mA
- ▶ Average Current: ~219.60 μ A
- ▶ Advertising Interval: ~100 ms
- ▶ Charge Consumption (10 s window): ~2.20 mC

Interpretation:

- ▶ The sharp spikes (~8–10 mA) represent TX bursts.
- ▶ The baseline (~1–2 μ A to hundreds of μ A depending on state) represents sleep/System ON idle between events.
- ▶ Average current is significantly influenced by advertising intervals
- ▶ shorter intervals drastically increase power consumption.

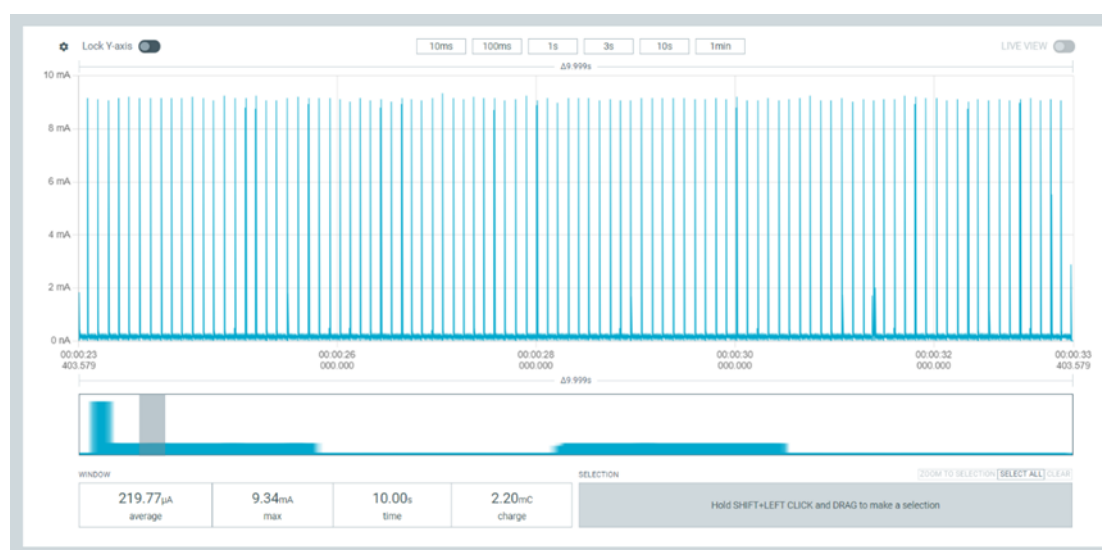


Figure 8 - BLE profile

11.3 Summary

Mode	Peak Current	Average Current	Notes
BLE Advertising@4dBm	~10 mA	~219 μ A	Dominated by TX bursts
System OFF	~10.52 μ A	~1.19 μ A	System OFF

Table 6 - Power Consumption

12. Reflow Diagram:

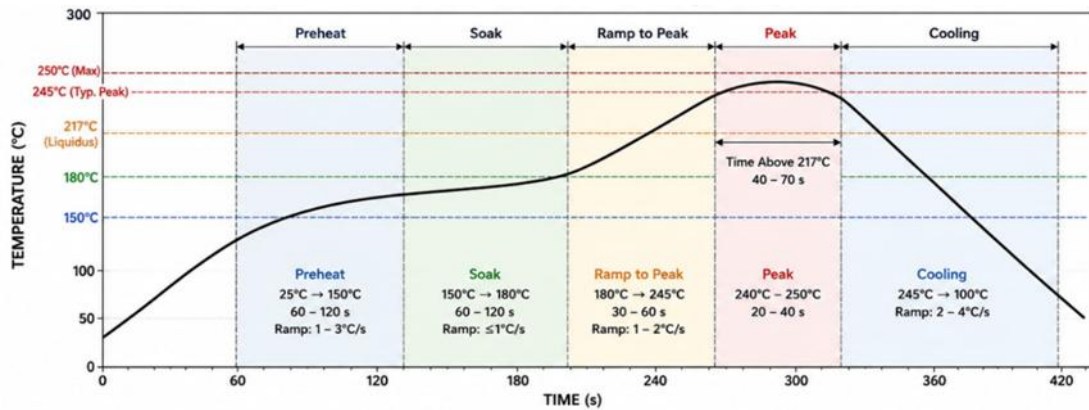


Figure 9 - Reflow Diagram

Stage	Temperature Range	Time Duration	Ramp Rate
Preheat	25°C → 150°C	60–120 sec	1–3°C/sec
Soak	150°C → 180°C	60–120 sec	≤1°C/sec
Ramp to Peak	180°C → 245°C	30–60 sec	1–2°C/sec
Peak Temp	240°C → 250°C	20–40 sec	—
Cooling	245°C → 100°C	—	2–4°C/sec

Table 7 - Reflow Rate

Wd

13. Regulatory Compliance:

The ISC-nRF54L15-A module has been certified to meet the following regulatory requirements.

Region	Certification	Identification
United States	FCC	FCC ID: 2BVP2-NRF54L15
European Union	CE	Certificate No.: BTFT657-EU
India	WPC	ETA No.: ETA-SD-20251009234

Table 8 - Certifications

14. FAQs:

► How To Program ISC Series of beacons & Module:

To program the IndieSemiC Range of Modules/Beacons, use the segger J-Link debugger. For development and testing purposes we have used NRF52840 DK for programming below is short guideline for it.

Make the following connections between the Nordic DK and the target module:

- **SWDIO → SWDIO**
- **SWDCLK → SWDCLK**
- **RESET → RESET**
- **VCC (3.3 V) → VCC**
- **GND → GND**
- **Short VDD_nRF and VTG (or SWDSL) on the DK to ensure the target receives correct reference voltage.**

After wiring, power the module through the DK and use nRF Connect for Desktop (Programmer app) or the nrfjprog command-line tool to flash firmware via SWD.

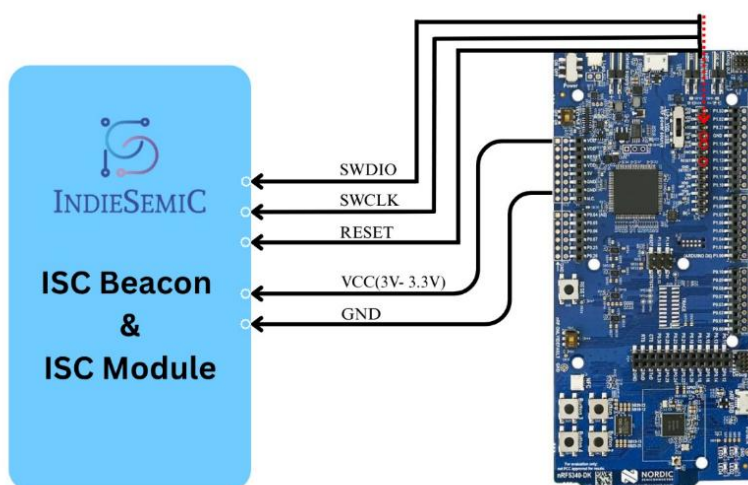


Figure 10 - Programming ISC series module

- For a wider range of RF modules and evaluation kits, or to find an evaluation kit for this module:
 Evaluation Kit: [EVK-ISC-nRF54L15-A](#)
 Other: [RF Modules](#)
- If you would like your schematic or Gerber files reviewed before Production, you can contact Nordic [DevZone](#)