Version update instructions:

version number	Change the time	Modify content	Edited by
V1.0	2014/01/22	create	HCJ
V1.01	2014/05/08	Add timing requirements for UART communication Add soft reset delay time description	HCJ
	2014/07/25	Modify the description of the power factor register, complement code Modify part of the error description	HCJ
V1.02	2015/06/18	Modify VAOS, RMS_CREEP, I_PKLVL, V_PKLVL Description	HCJ
V1.1	2015/11/20	Version upgrade and modification	HCJ
V1.11	22 November 2015	Modify part of the error description	HCJ

features

- High precision, within the input dynamic working range (6000:1) , the non-linear measurement error is less than 0.1%
- signal stability, I b point C Foutput jump is less than 0.01 %
- -signal stability, 0.0 2 % I b point C F jump less than 0 . 1 %
- chip can accurately measure the active power in both positive and negative directions, and output fast output pulses (CF)
- chip has two current sampling terminals, sampling live wire and neutral wire current
- chip gives the effective value of voltage and double current, and the measuring range (20mA~12Ib)
- chip has a double anti-creep design, ensuring that the In the creep experiment of 1 hour, no more than 1 pulse
- chip has the function of voltage loss and phase failure detection
- There is a power supply voltage monitoring circuit on the chip to detect power-off conditions
- chip has programmable gain adjustment and phase compensation
- factor (PF) measurement range (20mA~12Ib)
- chip has a built-in reference voltage source of 2.5V, and an external 2.5V voltage. There is a reference power-down detection inside to prevent the fast walk caused by the breakdown of the external capacitor.
- External crystal oscillator 3.58MHz
- Chip single working power supply 5V , low power consumption 25mW (typical value)
- BL6523GX is a UART interface chip, the communication rate is fixed at 4800bps

Related patent applications

overview

BL6523GX is a wide-range single-phase multi-function electronic energy metering chip, suitable for simple single-phase multi-function or single-phase power line carrier energy meter applications, with high cost performance.

BL6523GX integrates 3-way high-precision Sigma-Delta ADC, reference voltage, power management and other analog circuit modules, as well as digital signal processing circuits for processing electrical parameters such as active power, apparent power, and current and voltage RMS.

BL6523GX has two current sampling terminals, which respectively sample the current of live wire and neutral wire. When the difference between the two exceeds the set threshold, an indication signal is issued, indicating that there is electricity stealing or wrong wiring. It can realize dual-channel automatic monitoring according to the set threshold. switch.

BL6523GX can measure single-phase active energy, apparent energy, power factor, current and voltage effective value, line frequency and other parameters; it has the function of voltage loss and overvoltage monitoring; current and voltage peak detection ; Functional energy meter needs.

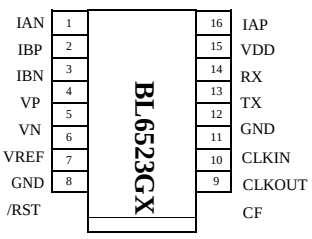
BL6523GX has a patented anti-creep design, and with reasonable external hardware design, it can pass the 0.5mT external strong magnetic field interference test . In addition, in the latent experiment of more than 48 hours, it is ensured that no large at 1 pulse.

BL6523GX integrates a UART interface. To facilitate the transmission of metering parameters and meter calibration parameters with the external MCU . The communication interface is specially designed with high reliability. The BL6523GX can be reset through the soft reset function to ensure reliable measurement.

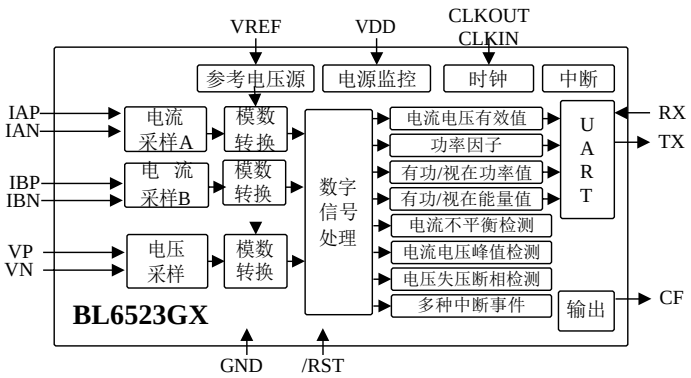
BL6523GX supports full digital domain offset compensation, gain adjustment , phase correction (up to ±0.635° adjustable) , etc. Active power calibration outputs fast pulse CF , which can be directly connected to the standard meter for error correction.

BL6523GX complies with the new national grid standard.

Pinout and System Block Diagram



SOP16

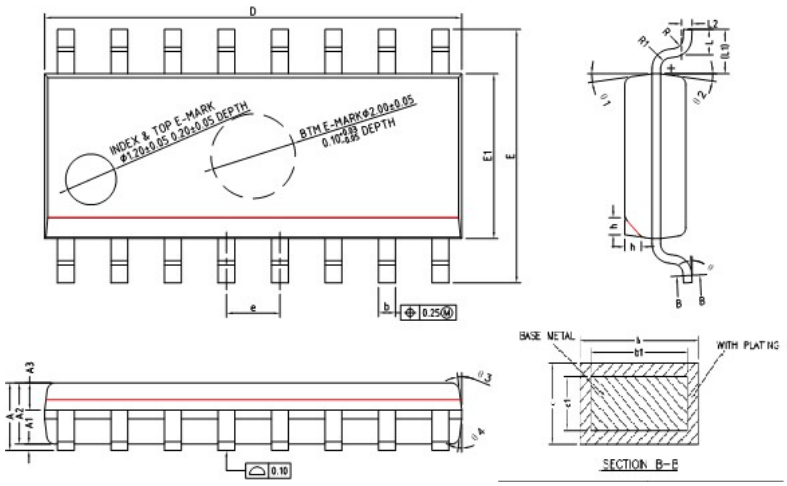


1. Pin definition （SOP16）

pin number	symbol	illustrate
16,1	IAP，IAN	The analog input of the current channel, the maximum differential voltage of the pins is ±660mV, the gain can be adjusted, see the register GAIN for details. Due to internal ESD Protection circuit if voltage overvoltage within ±1.5V , there will still not be too much damage.
2，3	IBP，IBN	The analog input of the current channel, the maximum differential voltage of the pins is ±660mV, the gain can be adjusted, See register GAIN for details. Due to the internal ESD protection circuit, if the voltage overvoltage is within ±1.5V, there will still not be too much damage.
4，5	VP，VN	The analog input of the voltage channel, the maximum differential voltage of the pin is ±660mV, see the register for details GAIN.(Same as above, the maximum signal amplitude is ±1.5V)
6	VREF	of the on-chip reference voltage is 2.5±8%, and the typical value of the temperature coefficient is 5ppm/°X. An external reference source can be connected to this pin. Alternatively, this pin needs to be used A 1uF ceramic capacitor eliminates coupling to ground.
7	GND	The internal analog circuit is referenced to ground. This pin should be bound to the analog ground plane or the most stable static ground in the system. This static ground is used in all analog circuits. In order to minimize the noise in the chip ground signal, the static ground plane can only be Connect digital horizon at one point noodle.
8	/RST	Chip reset signal input, active low.
9	CF	Calibration pulse output pin, this pin gives active power information, this output can be used to compare the meter, the output frequency at full scale can be adjusted by WA_CFNUM. When measuring low power, CF sets the pulse width to 90ms. When measuring high power, the CF output cycle is less than 180ms When , the pulse width of CF is half of the period.
10	CLKOUT	The crystal oscillator can provide the clock for the chip through this pin and the CLKIN pin. When external When clock and crystal oscillator are introduced, this pin can drive a CMOS load.

11	CLKIN	The main clock of the internal analog circuit and digital processing circuit can introduce an external clock. Crystal can be connected in parallel on CLKIN and CLKOUT Provide the clock source for the chip, the clock frequency is 3.58MHz. 22pF and 33pF can be used in crystal oscillator circuits.
12	GND	The internal analog circuit is referenced to ground.
13	TX	The data output terminal of the serial interface.
14	RX	Data input for the serial interface. RX pin multiplexing /RST reset function
15	VDD	Positive power supply (+5 V) provides analog part power supply, the power supply voltage should be kept at Between +4.5V~5.5V.

2. Package size SOP16



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
A3	0.55	0.65	0.75
b	0.36	–	0.51
b1	0.35	0.40	0.45
c	0.18	–	0.25
c1	0.17	0.20	0.23
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.22	1.27	1.32
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

3. limit range

（ T = 25 ° C)

project	symbol	extremum	unit
Power supply voltage VDD	VDD	-0.3 ~ +7	V
Analog input voltage (relative to GND)	IAP , IBP , VP	-6 ~ +6	V
Digital Input Voltage (relative to GND)	RX	-0.3 ~ VDD+0.3	V
Digital Output Voltage (relative to DGND)	CF , TX	-0.3 ~ VDD+0.3	V
Operating temperature	Topr	-40 ~ +85	℃
storage temperature	Tstr	-55 ~ +150	℃
Power Dissipation (SSOP24)	P	80	mW

4. Electrical parameters

（ VDD = 5V , GND = 0V , on-chip reference voltage source, 3.58MHz crystal oscillator, 25 ° C)

Measurement items	symbol	Measurement conditions	Measuring point	the smallest	typical	maximum	unit
Active Power Measurement Error (absolute error)	WATT_err	6000:1 input dynamic range	CF		0.1	0.3	%

Active power measurement bounce (big signal)	ΔIb _	Ib=5A input, test the average of 2 laps	CF		0.006	0.01	%
Active power measurement bounce (small signal)	Δ 0.02%Ib	0.02% Ib input, test 1 circle	CF		0.1	0.2	%
The phase angle between the channels causes Measurement error (capacitive)	PF08err	Phase lead 37 (PF=0.8)				0.5	%
The phase angle between the channels causes Measurement error (inductive)	PF05err	Phase lag 60 (PF=0.5)				0.5	%
AC Power Supply Rejection (Output output frequency amplitude change)	ACPSRR	IP/N=100mV			0.01		%

DC Power Supply Rejection (Output output frequency amplitude change)	DCPSRR	VP/N=100mV			0.1		%
Voltage RMS measurement Accuracy (relative error)	VRMSerr	0.4%Ib~12Ib input DR			0.3		%
Current RMS measurement Accuracy (relative error)	IRM Serr	0.4%Ib~12Ib input DR			0.3		%
Analog input level		Differential Input (Peak)				1200	mV
Analog input impedance					370		kΩ _
Analog input bandwidth		(-3dB)			14		kHz
Analog input gain error Difference		External 2.5V reference Voltage		-4		+4	%
Analog input phase increase benefit matching error		External 2.5V reference Voltage		-1.5		+1.5	%
Internal Voltage Reference	Vref		VREF		2.5		V
base deviation	Vreferr					± 200	mV
Temperature Coefficient	Temp Coef				5	15	ppm/ ℃
logic input high		VDD=5V ± 5%		2.6			V
Logic input low		VDD=5V ± 5%				0.8	V
logic output high		VDD=5V ± 5%		4			V
Logic output low level		VDD=5V ± 5%				1	V
Power supply VDD	VDD			4.5		5.5	V
AIDD	IAVDD	VDD=5.25V			3		mA
DIDD	IDVDD	VDD=5.25V			2		mA

5. Working principle

5.1 System Block Diagram

The current signal and the voltage signal are respectively converted into analog by gain amplifier (PGA) and high-precision analog-to-digital conversion (ADC).

the high-frequency noise and DC offset are filtered out through the down-sampling filter (SINC4) and high-pass filter (HPF) to obtain the required current waveform data and voltage waveform data .

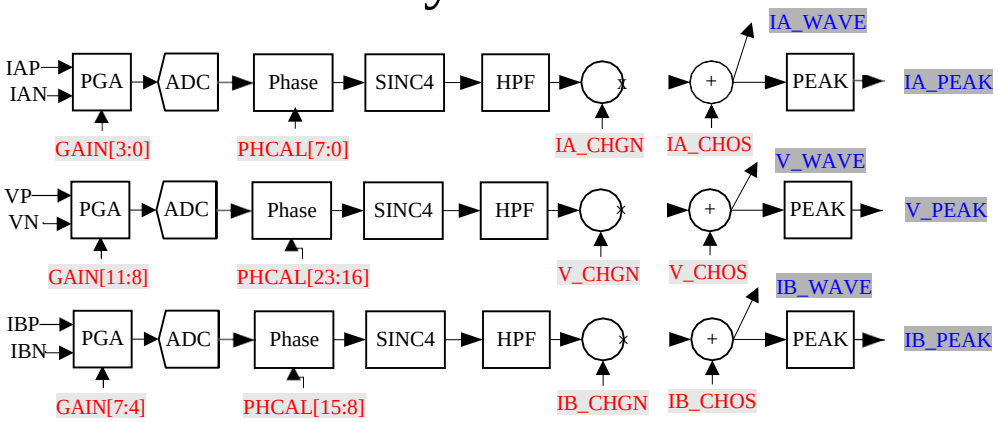
The instantaneous active power is obtained by multiplying the current waveform data and the voltage waveform data, and then passes through a low-pass filter (LPF1) the output average active power. Here the current channels are calculated separately A and current channel B average active power. Select one of the active power channels to obtain active energy through integration.

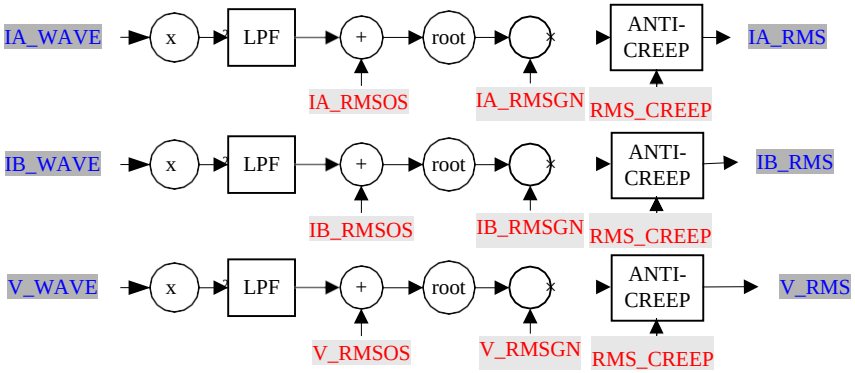
the voltage waveform data pass through the square circuit (X^2) the low-pass filter (LPF) and the root circuit respectively (ROOT) get current effective value and voltage effective value respectively.

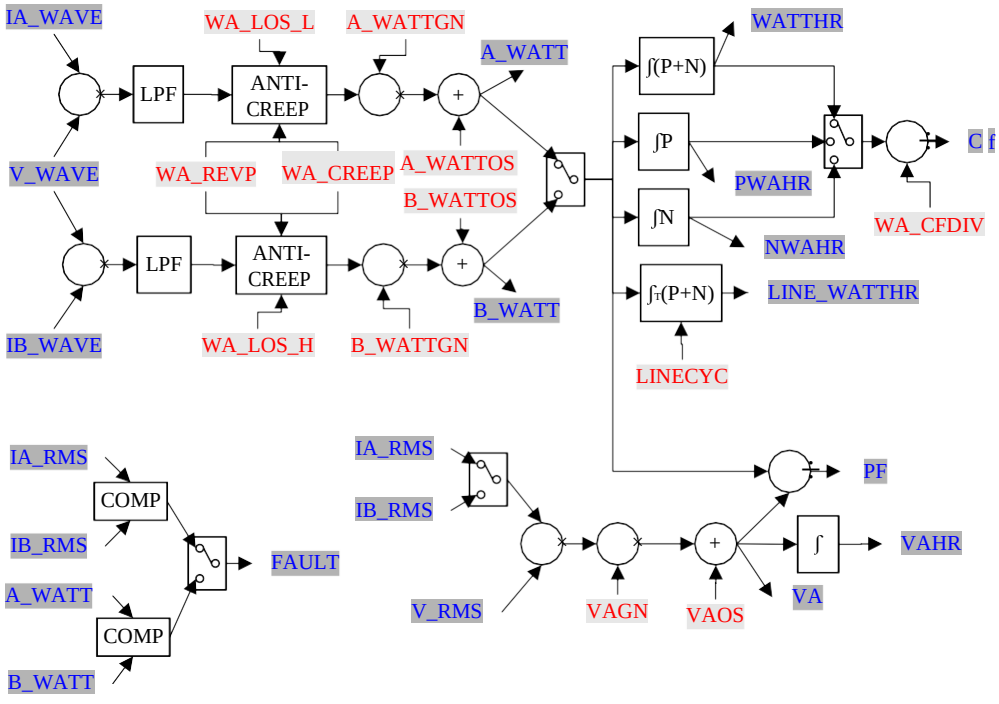
The product of the effective value of the current and the effective value of the voltage can obtain the apparent power, and the ratio of the active power to the apparent power is the power factor.

When the current RMS or active power of the A and B channels differ by a certain value, or the average active power of the A and B channels differ by a certain value, the FAULT signal is output to indicate the unbalanced state of the two phases.

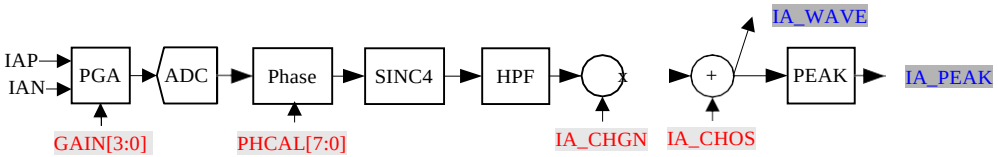
BL6523GX System block







5.2 Front-end waveform calculation



Front-end waveform calculation includes gain amplifier (PGA) high-precision analog-to-digital conversion (ADC) phase correction (PHASE) down-sampling filter (SINC4), high-pass filter (HPF) and channel gain adjustment modules to obtain the required current waveform data and voltage waveform data (IA_WAVE, IB_WAVE, V_WAVE) (above pictured with A channel current example)

5.2.1 Front-end gain adjustment

of BL6523GX has a programmable gain amplifier PGA, whose optional gain can be adjusted in 7 stages. Gain selection can be realized by writing to the gain register (GAIN), and the default value of GAIN is 000H.

The gain registers each use 4 bits to select the PGA of the current channel or the voltage channel. The current A channel uses bits [3:0], the current B channel uses bits [7:4], and the voltage V channel uses bits [11:8].

Such as current A channel, use [3:0] bits to adjust.

x000 = 1 times
x001 = 2 times
x010=4 times
x011=8 times
x100=16 times
x101=24 times
x110=32 times
x111 cannot be set

5.2.2 phase compensation

BL6523GX provides a method to digitally calibrate the phase error between current and voltage channels. It compensates the phase error between channels caused by external PCB layout and wiring by introducing a digitally settable time delay in the current channel or voltage channel. This method is only suitable for small phase errors in the range of ± 0.635°. Note that using time-shifting techniques to correct for large phase errors introduces significant phase errors in higher harmonics.

The phase calibration register (PHCAL) is a binary 24-bit register, where [7:0] compensation current A channel, [15:8] compensation current B channel, [23:16] compensation voltage V channel, the default value is 000000H. The highest bit in every 8 bits is the enable bit. Take the current A channel as an example, when [7] = 0, the compensation is turned off; when [7] = 1, the compensation is valid. Use [5:0] bits to fine-tune the delay time,

1LSB corresponds to 1 delay, up to 63 delays, each delay 0.5587us. For a 50Hz input signal, the resolution of the corresponding minimum phase compensation is 0.01°, and the maximum adjustable 0.635°.

5.2.3 Input bias correction

B L 6523 G X Also contains the input offset correction registers (IA_CHOS , IB_CHOS , V_CHOS) , these _ _ _ _ _ _ _ The default value of the 16 -bit register is 0000H . They use the data in the form of 2 's complement to eliminate the deviation caused by the analog-to-digital conversion of the current A channel, the current B channel and the voltage V channel. The deviation here may be derived from the offset generated by the input and the analog-to-digital conversion circuit itself . Offset correction can make the input waveform offset close to 0 under no-load conditions .

5.2.4 Channel Gain Correction

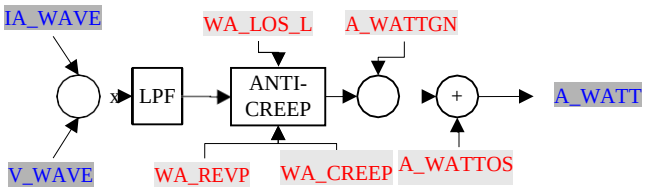
BL6523GX It also contains channel gain correction registers (IA_CHGN, IB_CHGN, V_CHGN) which are 16-bit signed numbers, and the default value is 0000H. They adjust the gain of the current A channel, current B channel and voltage V channel with data in 2's complement form, and the adjustable range is ± 50%.

$$output\ \ WAVE = WAVE \times (1 \pm \frac{CHGN}{2^{16}})$$

For example: write 7FFFH (hexadecimal) to IA_CHGN, the output waveform amplitude increases by 50%, because 7FFFH = 32767 (decimal) 32767/65535 = 0.5. Similarly, write 8001H When, the amplitude of the output waveform decreases 50%.

5.3 Active energy metering principle

The instantaneous active power is obtained by multiplying the current waveform data and the voltage waveform data, and then passes through a low-pass filter (LPF1) the output average active power. Here the current channels are calculated separately A and current channel B average active power. Select one of the active power channels to obtain active energy through integration. (The figure below takes channel A as an example)



5.3.1 Principle of active power calculation

Electric energy metering mainly multiplies the input voltage and current signals according to time to obtain the information of power changing with time. Assuming that the current and voltage signals are cosine functions and there is a phase difference Φ, the power is:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$

Order Φ=0:

$$p(t) = \frac{VI}{2}(1 + \cos 2(wt))$$

令Φ≠0时:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$
$$= V\cos(wt) \times [I\cos(wt)\cos(\Phi) + \sin(wt)\sin(\Phi)]$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + VI\cos(wt)\sin(wt)\sin(\Phi)$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + \frac{VI}{2}\sin(2wt)\sin(\Phi)$$

2 2

p(t) is called the instantaneous power signal, and the ideal p(t) only includes two parts: the DC part and the AC part with a frequency of 2ω. The former is also called instantaneous real power signal, and instantaneous real power is the primary object of electric energy meter measurement.

If the current and voltage signal is not a cosine function, the signal can be expanded into harmonics of the cosine function according to Fourier transform, and can also be calculated according to the above p(t)=v(t)*i(t), which will not be described in detail here.

5.3.2 Active power offset correction

Active power bias registers (A_WATTOS, B_WATTOS), yes 16 bit register, the default is 0000H. _ _ These registers start with 2 The two's complement representation of. A_WATTOS used to eliminate the adopted current A Deviation occurring in channel metered active power ; B_WATTOS used to eliminate the employed current B Deviations in the active power metered by the channel; the deviation here may be due to the PCB in the power calculation Crosstalk between two channels on the board and on the IC itself. Offset correction can bring the value in the active power register close to 0 at no load.

$$Active\ Power = ActivePower_0 + \text{WATTOS}$$ (see register description for detailed formula)

5.3.3 Active Power Gain Adjustment

The gain of active power can be adjusted through the gain register (A_WATTGN, B_WATTGN) to adjust the range of the active power measured by the current A channel and the active power measured by the circuit B channel respectively. This register is a 16 -bit signed number, and the default value is to 0000H. The following formula shows how the active power gain register is used for gain adjustment:

$$output\ \text{WG} = Active\ Power \times (1 \pm \frac{WG}{2^{15}})$$

For example: write 7FFFH (hexadecimal) in A_WATTGN, the power output will increase by 50%, because 7FFFH = 32767 (decimal) 32767/65535 = 0.5._Similarly, write 8001H When the power output decreases 50%.

B_WATTGN is used in the same way.

5.3.4 Active power anti-creep

BL6523GX includes two anti-creep methods: power threshold anti-creep and time threshold anti-creep.

Anti-creep Threshold Register (WA_CREEP) for twenty four bit. register is divided into two parts, the low 12 bit WA_CREEP_L sets a power anti-creep threshold in the form of an unsigned number, and the default is 02BH. When the absolute value of the input active power signal is less than this threshold, the output active power is set to zero. This makes the output to the active power register a value of 0 at no load, even with a small noise signal.

$$WATT = \begin{cases} 0 & , \ |WATT| < WA\_CREEP\_L \\ WATT, & |WATT| >= WA\_CREEP\_L \end{cases}$$

Anti-creep Threshold Register (WA_CREEP) High 12 bit WA_CREEP_H Set a timer threshold in the form of unsigned number, the default is FFFH. There is a timer register TIME_CREEP inside, and whenever a CF pulse output is detected,

the register TIME_CREEP is set to the value of WA_CREEP_H . If no CF pulse output is detected , the value of the TIME_CREEP register will decrement. If there is still no CF signal output when the TIME_CREEP register is decremented to 0 , the register TIME_CREEP will generate a clear signal to generate the internal energy accumulation register of the CF pulse . will be cleared. After clearing, the timer register TIME_CREEP still restores to the value of WA_CREEP_H , and starts counting again . WA_CREEP_H can be written or read by the user, the default value is FFFH, the resolution of this register is 4.6s/ LSB , so the maximum anti-creep time is about 5h06m . For example, WA_CREEP_H=216H , the corresponding anti-creep time threshold is 40 minutes, if there is no CF output within 40 minutes, the CF energy accumulation register will be cleared, and there will be no CF output. The timing anti-submarine mode is turned on when MODE[6]=1 , and closed when MODE[6]=0 ; the power threshold anti-submarine mode is always Work.

The timing anti-submarine method can be applied to the external strong magnetic field experiment of 0.5mT . First, the external hardware circuit design should ensure that under the strong magnetic field interference, the chip input interference power is less than the chip's normal startup power, and the timing anti-submarine time is set to be greater than the normal startup time. And leave a certain margin, it can pass the 0.5mT external strong magnetic field experiment. It can also be applied to long-term anti-submarine, to ensure that no more than one pulse will occur in any length of submersion test.

5.3.5 Small Signal Compensation of Active Power

B L 6523 G X contains an active power small- signal compensation register (WA_LOS), the twenty four bit register with 2 's complement form of data to compensate the active power error when inputting a small signal. high 12 bit compensation B Phase power, where [23] is the sign bit, and the lower 12 bits compensate A Phase power, where [11] is the sign bit, and the default value is 000000H .

5.3.6 reverse indication threshold

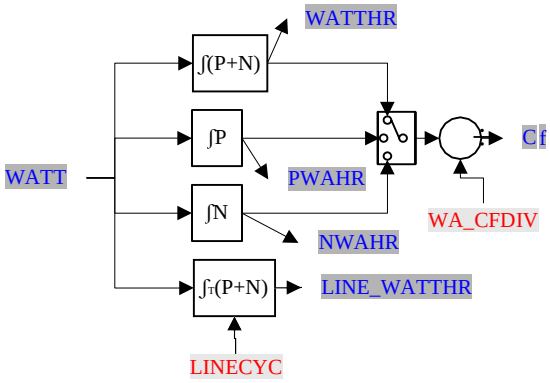
B L 6523 G X contains a reverse indication threshold register (WA _ R EV P), the 12 The bit register sets a threshold in the form of an unsigned number. When the input active power signal is negative and the absolute value is greater than this threshold, the output reverse indication REVP . This register only affects STATUS[6] (REVP flag bit) , and does not affect the sign bit of A_WATT and B_WATT registers. The /IRQ logic output becomes active low if the corresponding REVP enable bit in the interrupt mask register (MASK) is logic 1 (applicable to BL6523G) ;

The sign bit of the average power register or the real-time power sign bit can be selected by setting MODE[19] as

Reverse indication of STAUTS[6] .

5.4 energy calculation

Active power can be obtained by integrating active energy.



5.4.1 Principles of Energy Calculation

The relationship between power and energy can be expressed as:

$$Power = \frac{energy}{dt}$$

The reverse is :

$$Energy = \int Power\ dt$$

In BL6523GX , active energy is obtained by continuously accumulating active power signals in a 53 -bit internal register , and the active energy register WATTHR[23:0] takes

out the upper 24 bits of this internal register as active energy output. Here the continuous accumulation of discrete signals is the same as the integration of continuous signals, namely:

$$E = \int p(t)\,dt = Lim_{\substack{T\to 0 \\ n=0}} \{ \sum P(nT) \times T \}$$

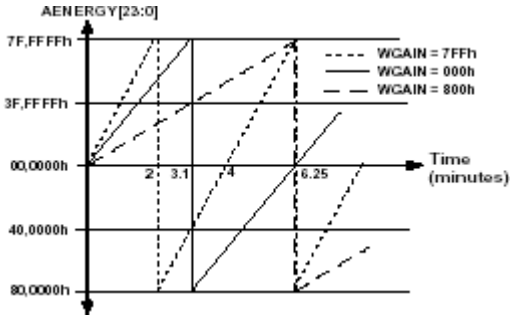
Here n is the number of samples, T is the sampling period, and the active power sampling period T is 1.1us.

In this way, accumulating the power signal can also eliminate the unfiltered AC signal in the power signal. active power signal

The number is continuously accumulated in the internal active power register.

The power signal WATT enters the 55- bit internal integrator for superposition, and then writes the high 24 of the internal register into the active energy register (WATTHR). When the input is full-scale, the register overflow time is about 10 minute. When the highest bit of the active energy register (WATTHR) is 1 , a half-full indication APEHF is given , if the corresponding 1 in the APEHF enable bit causes the /IRQ logic output to become active low.

The figure below shows the accumulation of the active energy signal in the internal register at full scale of the analog input:



5.4.2 Calculation principle of line cycle energy

Similarly, BL6523GX Line Energy Register (LINE_WATTHR) at LINECYC The register sets the line cycle accumulation time, 20mS/LSB . In the set n line periods, the power signal WATT enters the 32 -bit internal integrator for superimposition, and then the high value of the internal register twenty four Write to Line Cycle Energy Register (LINE_WATTHR). After that, the LINE_WATTHR register is refreshed every n line cycles.

Line cycle energy accumulation is mainly used for quick meter calibration.

5.4.3 Forward active energy calculation

The relationship between forward power and forward energy can be expressed as:

$$PWATT = \frac{d(PWAHR)}{dt}$$

The reverse is :

$$PWAHR = \int (PWATT)\, dt$$

In BL6523GX , the forward active energy is obtained by continuously accumulating the positive active power signal in a 49 -bit internal register, and the forward active energy register PWAHR [23:0] takes out the upper 24 bits of this internal register as the positive Active energy output. Here the continuous accumulation of discrete signals is the same as the integration of continuous signals, namely:

$$E = \int_{0}^{\infty} p(t)\, dt = Lim_{T \to 0} \{ \sum_{n=0} P(nT) \times T \}$$

Here n is the number of samples, T is the sampling period, and the sampling period T in BL6523GX is 1.1us.

In this way, accumulating the power signal can also eliminate the unfiltered AC signal in the power signal. The positive power signal WATT enters the 49 -bit internal integrator for superposition, and then writes the high 24 of the internal register into the positive active energy register (P W AH R), and the register overflow time is about 10 minute.

5.4.4 Reverse active energy calculation

Similarly, the relationship between reverse power and reverse energy can be expressed as:

$$NWATT = \frac{d(NWAHR)}{dt}$$

The reverse is :

$$NWAHR = \int NWATT\, dt$$

In BL6523GX , the reverse active energy is obtained by continuously accumulating the reverse active power signal in a 49 -bit internal register, and the reverse active energy register NWAHR[23:0] takes out the upper 24 bits of this internal register as the reverse Active energy output.

The reverse power signal WATT enters the 49 -bit internal integrator for superposition, and then writes the high 24 of the internal register into the reverse active energy register (WAHR_N), and the register overflow time is about 10 minute.

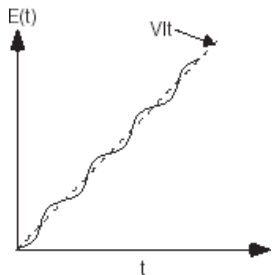
5.4.5 frequency output

For calibration, BL6523GX also provides energy frequency conversion. In addition to the initial calibration of the manufacturer, end users also need to frequently calibrate the energy meter. For manufacturers, the most common method used for calibration is to generate a (energy) proportional to the pulse output. This pulse output can be connected to external calibration equipment through a simple, single-wire, optically isolated port .

BL6523GX You can choose to output active energy accumulation (WATTHR), positive energy accumulation (PWAHR), negative energy accumulation (NWAHR), and then according to CF The coefficient provided by the scaling register (WA_CFDIV) generates a CF pulse output through digital-to-frequency conversion, and CF needs a fixed pulse width of 90ms . Under the condition of stable load, the output frequency is proportional to the active power. When the AC input is full scale and WA_CFDIV=010H , the maximum output frequency is about 0.5kHz .

BL6523GX uses a register (WA_CFDIV) to set the frequency of CF. This 12 -bit unsigned register can adjust the CF frequency in a wide range , and the default value is 001H . When WA_CFDIV[x] is set to 1 , its zoom ratio is (2^(x- 4))

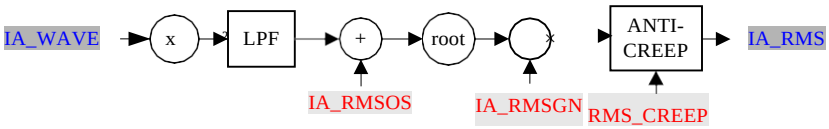
Since the filter cannot be completely ideal, the signal after the low-pass and even after the DFC will contain the Sin(2wt) component . The figure below shows the energy change curve with time, and the dotted line is the ideal active energy curve. It is equal to V × I × t , and the actual energy curve is a real curve, because the average value of the sinusoidal signal is zero, so the sinusoidal ripple will not affect the



accumulation of the energy signal. However, these sinusoidal ripples can be observed in the output frequency, especially at higher frequencies. The greater the load and the higher the frequency, the more pronounced this sinusoidal ripple will be. This is because the higher the frequency, the shorter the time for signal accumulation and averaging during energy frequency conversion, and the more obvious the sinusoidal change. Therefore, choosing a relatively low frequency output can greatly reduce the influence of the sinusoidal variation phenomenon, which is beneficial to pulse calibration. Also, the same effect can be obtained by averaging the output frequency with a longer clock gate time .

5.5 RMS calculation

the voltage waveform data pass through the square circuit（X²）the low-pass filter（LPF）and the root circuit respectively
（ROOT）get current effective value and voltage effective value respectively.



5.5.1 RMS calculation principle

The effective value is also the root mean square of the signal（Root Mean Square—RMS）the root mean square of a continuous signal is calculated as follows:

$$V_{rms}=\sqrt{\frac{1}{T}\int_0^T V^2(t)dt}$$

For discrete digital signals, the formula becomes:

$$V_{rms}=\sqrt{\frac{1}{N}\sum_{i=1}^{N}V^2(i)}$$

5.5.2 RMS deviation correction

BL6523GX Contains RMS offset registers（IA_RMSOS, IB_RMSOS and V_RMSOS）these _
The default value of the 16-bit register is 0000H. They use 2's complement data to eliminate the current A channel, current
The deviation that occurs in the RMS calculation of the B channel and the voltage V channel. This deviation may come from input noise, since there is a squaring step in calculating the rms value, which may introduce a dc offset due to noise. Offset correction can make the value in the rms register close to 0 at no load.

The calibration method of the IRMSOS register in the channel is as follows, taking the current channel A as an example:

$$I_{ARMS}=\sqrt{I_{ARMS0}^2+IA\_RMSOS\times 2^{13}}$$

Here I_{ARMS0} It is the current RMS value before correction. The calibration method of the IB_RMSOS and V_RMSOS registers is the same as above.

5.5.3 RMS gain adjustment

The effective value gain can be adjusted through the effective value gain registers（IA_RMSGN, IB_RMSGN and V_RMSGN）to adjust the range of effective values. These registers are 16-bit signed numbers, and their default value is 0000H., like the active power gain registers, they adjust the gain of the effective value of the current A channel, current B channel and voltage V channel respectively.

For example: write 7FFFH in V_RMSGN, the effective value output of the voltage V channel will increase by 50%, write
8001H, the effective value output of the voltage V channel is reduced by 50%.

5.5.4 RMS measurement threshold

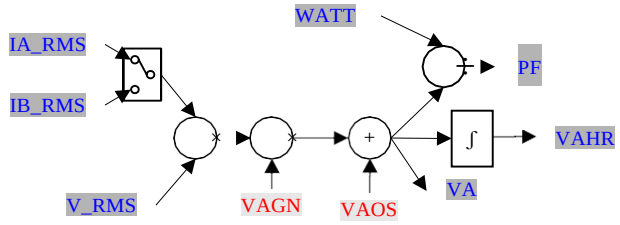
The effective value measurement threshold register RMS_CREEP can be set to limit the lower limit of the effective value measurement.

When the input effective value is less than this threshold (the value is automatically enlarged by 4 times) , the output effective value is set to zero. This allows the output to the rms register to be 0 at no load, even with a small noisy signal .

$$\text{RMS} = \begin{cases} 0 & |RMS| < RMS\_CREEP \times 2^{2} \\ \text{RMS}, & |RMS| >= RMS\_CREEP \times 2^{2} \end{cases}$$

5.6 Apparent power and energy calculation

The product of the effective value of the current and the effective value of the voltage can obtain the apparent power, and the ratio of the active power to the apparent power is the power factor.



5.6.1 Apparent Power Calculation

The apparent power is obtained by multiplying the effective value of current and the effective value of voltage.

$$VA = I\_RMS \times V\_RMS \_ \_ \_ \_$$

5.6.2 Apparent energy calculation

The apparent energy is obtained by integrating the apparent power, that is:

$$VA\_Energy = \_ \_ \int VA\ Power\ (t)\ dt$$

In BL6523GX , the apparent energy is obtained by continuously accumulating the apparent power signal in a 49 -bit internal register, and the upper 24 bits of this internal register are stored in the apparent energy register VAHR[23:0] . Here the continuous accumulation of discrete signals is the same as the integration of continuous signals, namely:

$$VA\_Energy = Lim_{T \to 0} \{ \sum_{n=0}^{\infty} VA\_Power \_ \_ \_ (nT) \times T \}$$

Here n is the number of samples, T is the sampling period, and the sampling period T in BL6523GX is 1.1us .

The apparent power signal is continuously accumulated into the internal register, where the accumulation is still a signed addition. The apparent energy register (VAHR) overflow time is about 10 minutes.

the highest bit of the apparent energy register (VAHR) is 1 , a half-full indication VAPEHF is given, and if the corresponding VAPEHF enable bit in the interrupt mask register is logic 1 , the /IRQ logic output becomes active low.

5.6.3 power factor

The power factor is obtained by dividing the active power by the apparent power.

$$PF = \frac{WATT}{VA}$$

PF register is a signed number, then 24'h7FFFFF means power factor = 1, 24'h800000 means power factor = -1, 24'h400000 means power factor = 0.5.

$$PF = (\text{sign bit}) \times \left(PF[22] \times 2^{-1} + PF[21] \times 2^{-2} + PF[20] \times 2^{-3} + \ldots + PF[1] \times 2^{-22} + PF[0] \times 2^{-23} \right)$$

5.6.4 Apparent Power Offset Correction

Apparent Power Offset Register (VA OS), is 1 6 bit register, the default is 000 0 H , with 2 The two's complement representation of . VAOS is used to eliminate the bias in the calculation of apparent power. Offset correction can bring the value in the apparent power register close to 0 at no load .

$$VA = VA_0 + \mathrm{VAOS}$$

5.6.5 Apparent Power Gain Adjustment

The gain of apparent power can be adjusted through the gain register VAGN to adjust the range of active power. The following formula shows how the apparent power gain register is used for gain adjustment:

$$output\ \ \mathrm{VA} = VA_0 \times (1 + \frac{\mathrm{VAGN}}{2^{16}})$$

5.7 Working mode selection

5.7.1 Power selection for energy accumulation

BL6523GX adopts dual current sampling and measures two-phase power at the same time. By default, the power of phase A is used for energy accumulation, and the output is CF. The MODE[0] of the working mode register (MODE) can be written by the user. When MODE[0] = 0 , the power of phase A is used for measurement; when MODE[0] = 1 , the power of phase B is used for measurement.

The MODE[1] of the working mode register (MODE) can be written by the user. When MODE[1] = 0 , when the unbalance of the two channels A and B is detected , the switching will not be performed automatically. At this time, the user writes the MODE The value of [0] determines whether to measure by channel A or channel B ; when MODE[1] = 1 , when it detects that the two channels of A and B are unbalanced, it will automatically switch , and the channel with the larger value will be used as the measurement channel , the imbalance judgment threshold is set by MODE[11:10] . For details, see Chapter 5.7.4 ″ Unbalance Judgment″.

5.7.2 High-pass filter use selection

After the analog-to-digital conversion circuit of BL6523GX , there are high-pass filters in the current and voltage channels to eliminate offset . The MODE[4： 2] of the working mode register (MODE) can be input by the user, and the default is 0 , which means high-pass filter is used. The high-pass filter needs to be turned on when measuring AC signals.

When MODE[2] = 0 , the current of channel A passes through the high-pass filter; when MODE[2] = 1 , the current of channel A does not pass through the high-pass filter. Similarly, when MODE[3] = 0 , the current of channel B passes through the high-pass filter; when MODE[3]
= 1 , the current of channel B does not pass through the high-pass filter.
Similarly, when MODE[4] = 0 , the voltage passes through the high-pass filter;

when MODE[4] = 1, the voltage does not pass through the high-pass filter.

5.7.3 Energy accumulation mode selection

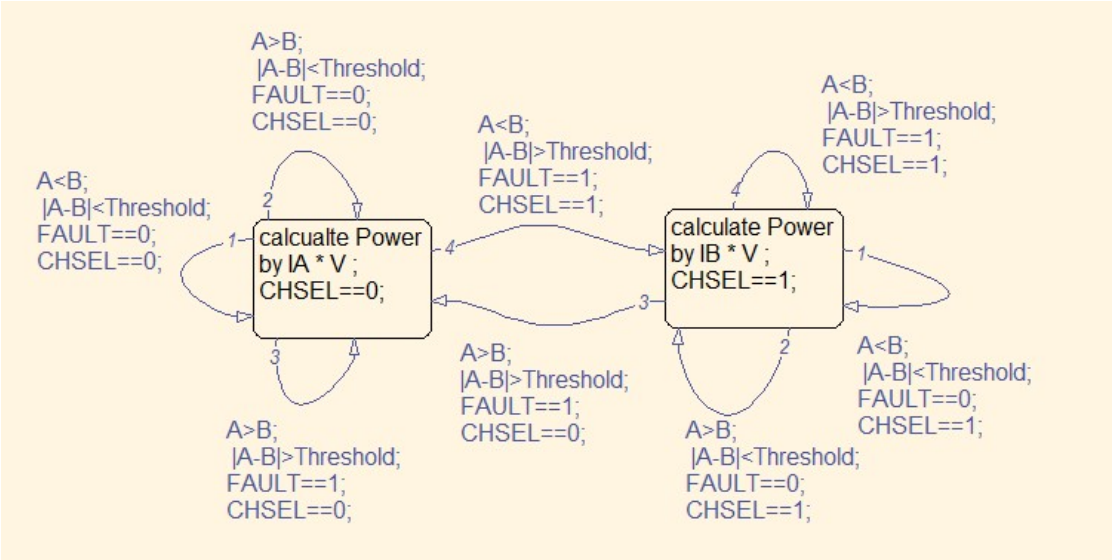
The MODE[9：8] of the working mode register（MODE）can be written by the user, and the default is 2'b00, which means that the energy accumulation mode adopts absolute value accumulation, and at this time the CF output corresponds to the energy accumulated by the absolute value. When MODE[9：8] = 2'b01, it means accumulating positive work, at this time CF outputs the energy corresponding to the accumulated positive work. When MODE[9：8] = 2'b10, it means that the energy accumulation mode adopts algebraic sum accumulation, and at this time CF outputs the energy corresponding to algebraic sum accumulation. MODE[9：8] = 2'b11, which means accumulating negative work, at this time CF output corresponds to the accumulated energy of negative work.

5.7.4 unbalanced judgment

B L 6523 G X The package can set the imbalance comparison threshold. Operating MRegister（MODE) of the M O DE [1 1：

10] can be written by the user, the default is 2'b00 , which means that the unbalanced judgment threshold is 12.5% , when the difference between the effective value of the sampling current of the live line and the neutral line or the difference between the two-phase power exceeds the set threshold , and output the wrong electricity indication signal FAULT . The /IRQ logic output goes active low if the corresponding FAULT enable bit in the interrupt mask register (MASK) is logic 1 . When MODE[11:10]=2'b11 , it means the threshold = 10.1 %; when MODE[11:10]=2'b10 , it means the threshold= 3.125 %; when MODE[11:10]=2'b01 , it means the threshold = 6.25 %; when MODE[11:10]=2'b00 , it means the threshold value = 12.5 %.

The specific switching process is as follows:



5.7.5 Channel imbalance detection mode selection

The MODE[5] of the working mode register (MODE) is the channel unbalance detection mode selection, the default is 1'b0 , use the current RMS value of A and B channels to compare the unbalanced state of power consumption; when it is 1 , use A phase Power and B -phase power to compare the unbalanced state of power consumption; in the two comparison methods, the comparison threshold and channel switching method are the same

5.7.6 Anti-creep mode selection

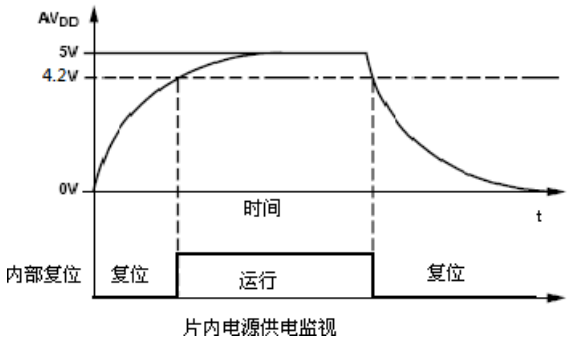
The MODE[6] of the working mode register (MODE) is the anti-creep mode selection, the default is 1'b0 , and the power threshold comparison method is used to prevent creep; when it is 1 , the timing anti-creep mode is turned on;

5.8 Electrical parameter monitoring

5.8.1 Power Supply Monitoring

B L 6523 G X contains an on-chip power monitoring circuit capable of continuous detection of analog power (AVDD) If the supply voltage is less than

4.2V ± 5%, then BL6523GX is not activated (does not work) that is, when the supply voltage is less than 4.At 2V, the chip is in reset state. This practice ensures that the device maintains correct operation when the power supply is turned on and off. The power monitoring circuit has a hysteresis and filtering mechanism that can largely eliminate false triggers due to noise. Generally, the decoupling part of the power supply should ensure that the ripple on AVDD does not exceed 5V ± 5% .



5.8.2 Zero-crossing detection

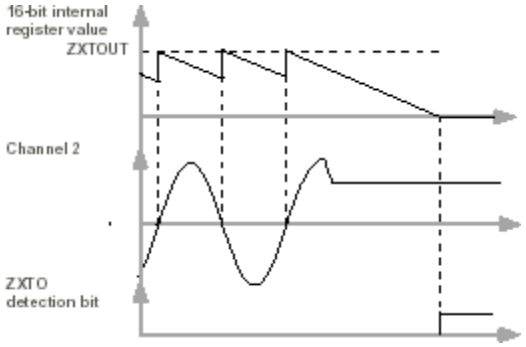
BL6523GX has a zero-crossing detection circuit in the voltage channel, when the voltage crosses zero from negative to positive, it outputs a zero-crossing signal ZX. A valid interrupt request /IRQ is output if the corresponding ZX bit in the interrupt mask register (MASK) is also set to logic 1. Interrupts are only generated from negative to positive zero crossings.

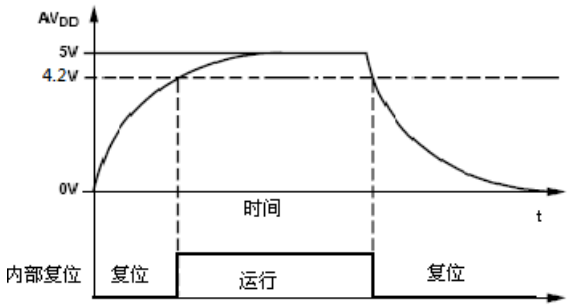
5.8.3 zero timeout

The zero-crossing detection circuit is also connected to a register ZXTOUT that detects the timeout of the zero-crossing signal. Whenever the detection voltage channel has a zero-crossing signal, ZXTOUT is set to the initial value. If there is no zero-crossing signal, it will be decremented. If there is no zero-crossing signal output for a long time, the value in this register will become 0. At this time, the corresponding bit ZXTO in the interrupt status register is set to 1. If the interrupt mask register When the corresponding enable bit ZXTO in is also 1, the zero-crossing signal timeout event will also be reflected on the interrupt pin /IRQ. Regardless of whether the corresponding enable bit in the interrupt register is set or not, the ZXTO flag bit in the interrupt status register (MASK) is always set to active 1 when the ZXTOUT register is decremented to 0.

The zero-crossing timeout register ZXTOUT can be written or read by the user, and the initial value is FFFFH. The resolution of this register is 70.5us/ LSB, so the maximum delay time of an interrupt is limited to 4.369s.

The figure below shows the mechanism for detecting zero-crossing timeout when the line voltage is always a fixed DC signal:

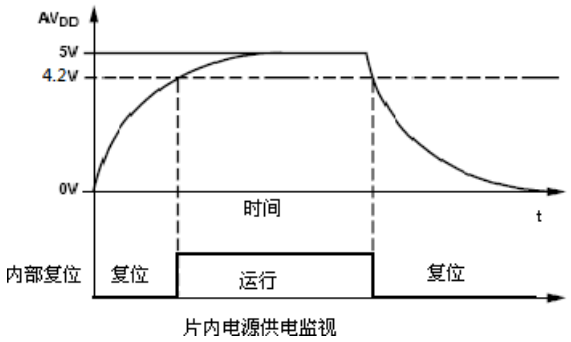




片内电源供电监视

5.8.4 Line voltage drop detection

BL6523GX can be programmed to indicate that when the effective value of the line voltage is lower than a certain peak value for more than a certain number of half cycles, it will give a line voltage drop indication.



片内电源供电监视

As shown in the figure above, when the effective value of the voltage is less than the threshold set in the drop voltage threshold register (SAGLVL) and the drop time exceeds the set time in the drop line cycle register (SAGCYC) (shown as exceeding the sixth half cycle, S AG C Y C [7 : 0] = 0 6 H), the line voltage drop event is set by setting the interrupt status register S A G flag to record . The /IRQ logic output becomes active low if the corresponding SAG enable bit in the interrupt mask register (MASK) is logic 1 .

The drop voltage threshold register (SAGLVL) can be written or read by the user, the initial value is FFFH . The drop line cycle register (SAGCYC) can also be written or read by the user, and the initial value is FFH . The resolution of this register is 10ms/ LSB , the maximum delay time of such an interrupt is limited to 2.55s .

5.8.5 peak detection

BL6523GX can record the maximum absolute value of the current channel and the voltage channel, which are stored in the current A transient peak register (I A _ P E A K), current B transient peak register (I B _ P E A K)and voltage transient peak register (V _ P E A K) . These three registers are 24 -bit unsigned numbers. Refresh frequency 100Hz .

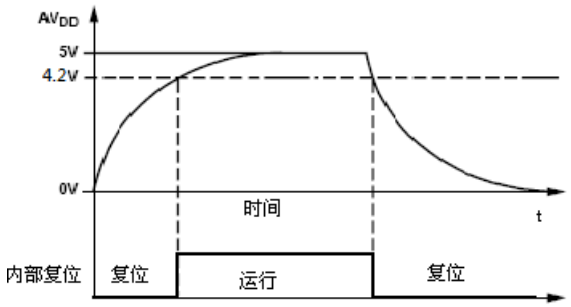
5.8.6 Current and voltage overload monitoring

BL6523GX can be programmed to set the threshold value of the current and voltage RMS, by the peak threshold register (I_PKLVL , V_PKLVL) setting.

When the current RMS value of channel A is greater than the threshold set by the current peak threshold (I_PKLVL) , the current overload indication PKIA is given, and if the corresponding PKIA enable bit in the interrupt mask register (MASK) is logic 1 , the /IRQ logic output becomes active low.

Similarly, when the current RMS value of channel B is greater than the threshold set by the current peak threshold (I_PKLVL) , the current overload indication PKIB is given, and if the corresponding PKIB enable bit in the interrupt mask register (MASK) is logic 1 , then /IRQ logic output goes active low.

Similarly, when the voltage RMS is greater than the threshold set by the voltage peak threshold (V_PKLVL) , a voltage overload indication PKV is given,



and if the corresponding PKV enable bit in the interrupt mask register (MASK) is logic 1, the /IRQ logic output output becomes active low.

Note: /IRQ logic output is only applicable to BL6523G.

5.9 to interrupt

are indicated by the Interrupt Status Register (STATUS).

the interrupt status register (STATUS) are automatically cleared after a read operation,

5.10 Serial communication interface UART (BL6523GX)

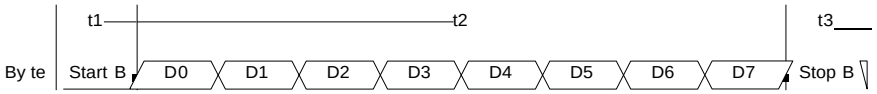
BL6523GX adopts UART communication mode. The UART interface only needs two low-speed optocouplers to realize isolated communication.

4800bps work. All communication is initiated by MCU sending commands to BL6523GX.

BL6523GX works in slave mode, half-duplex communication.

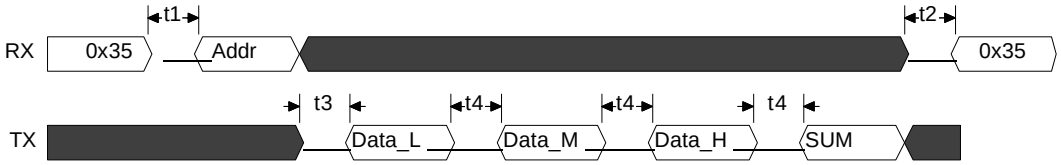
UART port settings: communication baud rate 4800bps, no parity, stop bit 1;

format per byte



t1=t3=208uS; t2=208*8=1664uS.

The operation flow of reading register data is as follows:

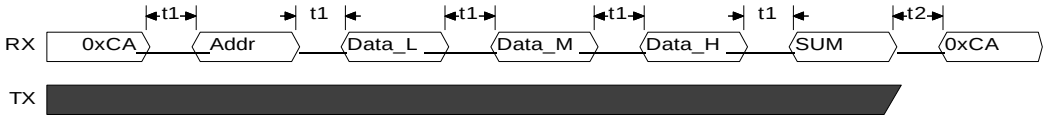


0x35 is the frame identification byte of the read operation;

Addr is the internal register address of BL6523GX corresponding to the read operation ;

The SUM byte is （ Addr+Data_L+Data_M+Data_H ） &0xFF inversion;

The operation flow of writing register data is as follows:



0xCA is the frame identification byte of the write operation;

Addr is the internal register address of BL6523GX corresponding to the write operation ;

The SUM byte is （ Addr+Data_L+Data_M+Data_H ） &0xFF inversion;

	illustrate	Min	type	Max	unit
t1	Interval time between MCU sending bytes	0		20	M
t2	Interframe time	0.5			u
t3	the MCU sending the register address during the read operation until BL6523GX sends bytes		72		u
t4	Interval time between bytes sent by BL6523GX		116		u

UART interface parameters:

Communication baud rate: 4800bps ± 10%

UART interface:

UART of BL6523D The communication provides a timeout protection mechanism. If the interval between bytes exceeds 22.68mS , the UART The interface resets automatically.

If the frame identification byte 0x35/0xCA is wrong or the SUM byte is wrong, the frame data is discarded.

UART module reset: RX pin is pulled high after the low level exceeds 6.52mS , and the UART module is reset.

5.11 reset function

5.11.1 RST pin reset

The RST pin is pulled down for more than 32uS, and the chip is reset after being pulled up for 300uS;

5.11.2 RX Pin multiplexing reset

The RX pin detects a continuous 20mS low level, and the chip resets after RX is pulled high for 300uS;

5.11.3 command reset

300uS to reset the chip after writing the soft reset command; see soft reset setting SOFT_NRST for details;

6. Register

6.1 register list

address	name	external read / write	internal read / write	bit number	default value	describe
Electrical parameter register (internal write)						
01H	IA_WAVE	R	W	twenty four	0	Current A waveform register, complement code, refresh rate 14KHz
02H	IB_WAVE	R	W	twenty four	0	Current B Waveform Register, Complement Code, Refresh Rate 14KHz
03H	V_WAVE	R	W	twenty four	0	Voltage V waveform register, complement code, refresh rate 14KHz
04H	LINE_ WATTHR	R	W	twenty four	0	Line Cycle Accumulated Active Energy Register
05H	IA_RMS	R	W	twenty four	0	Current A RMS register, refresh rate 2.5Hz
06H	IB_RMS	R	W	twenty four	0	Current B RMS register, refresh rate 2.5Hz
07H	V_RMS	R	W	twenty four	0	Voltage V RMS register, refresh rate 2.5Hz
08H	PF	R	W	twenty four	0	Power factor register, refresh rate 2.5Hz

09H	FREQ	R	W	twenty four	0	Line Voltage Frequency / Period Register
0AH	A_WATT	R	W	twenty four	0	current A channel metering device, complementary code, refresh rate 2.5Hz
0BH	VA	R	W	twenty four	0	Average apparent power register, refresh rate 2.5Hz
0CH	WATTHR	R	W	twenty four	0	active energy register
0DH	VAHR	R	W	twenty four	0	Apparent Energy Register
0EH	PWAHR	R	W	twenty four	0	positive energy register
0FH	NWAHR	R	W	twenty four	0	Negative energy register
10H	IA_PEAK	R	W	twenty four	0	Current A Transient Peak Register, Refresh Rate 100Hz
11H	IB_PEAK	R	W	twenty four	0	Current B transient peak register, refresh rate 100Hz
12H	V_PEAK	R	W	twenty four	0	Voltage V Transient Peak Register, Refresh Rate 100Hz
13H	B_WATT	R	W	twenty fo	0	current B channel metering device, complementary code, refresh rate 2.5Hz

				ur		
Calibration register (external write, except 3AH)						
14H	MODE	R/W	R	twenty four	000000h	Working mode register, see "Working Mode Selection" for details select" instructions
15H	GAIN	R/W	R	12	000H	Gain register, see "Front-end Gain Adjustment" for details illustrate
16H	FAULTLVL	R/W	R	12	044H	current or two-phase power imbalance mask threshold register (internal multiplier 2^8) compare the selected valid values or power comparison, the value of this register is different,

						Need to reset;
17H	WA_CREEP	R/W	R/W	twenty four	FFF02BH	The lower 12 bits are the anti-creep power threshold register (Internal times 2^4, the value is equal to 20ppm, the maximum F FF equal 0.2 %). The upper 12 bits are the anti-creep time threshold register, which is an unsigned number;
18H	WA_REVP	R/W	R	12	087H	reverse indication threshold register (internal times 2^8, the value is equal to 0.1 %, the maximum FFF00 is equal to 3 %)
19H	WA_CFDIV	R/W	R	12	001H	Active CF Scaling Register
1AH	A_WATTOS	R/W	R	16	0	A channel active power offset calibration register, complement code
1BH	B_WATTOS	R/W	R	16	0	B channel active power offset calibration register, complement code
1CH	A_WATTGN	R/W	R	16	0	A channel active power gain adjustment register, complement code
1DH	B_WATTGN	R/W	R	16	0	B channel active power gain adjustment register, complement code
1EH	FREQ_SEL	R/W	R	16	4924H	Analog circuit frequency control register. Customers do not need use.
1FH	BG_CTRL	R/W	R	twenty one	00FA3h	Analog circuit control register.
20H	P HC A L (contains IA_PHCAL , IB_PHCAL , V_PHCAL)	R/W	R	twenty four	0	Channel phase correction registers: 1. The lower 8 bits [7:0] are the current A channel phase correction register IA_PHCAL 2. The middle 8 bits [15:8] are the current B channel phase correction register IB_PHCAL 3. The upper 8 bits [23:16] are the voltage V channel phase calibration

						Positive register V_PHCAL
21H	VAOS	R/W	R	16	0	Apparent Power Offset Calibration Register, Two's Complement
22H	VAGN	R/W	R	16	0	Apparent power gain adjustment register, two's complement
23H	IA_RMSGN	R/W	R	16	0	Current A RMS gain trim register, two's complement,
24H	IB_RMSGN	R/W	R	16	0	Current B RMS gain trim register, two's complement,
25H	V_RMSGN	R/W	R	16	0	Voltage V RMS gain trim register, two's complement,
26H	IA_RMSOS	R/W	R	16	0	Current A RMS offset correction register, two's complement, internal *4 ;
27H	IB_RMSOS	R/W	R	16	0	Current B RMS offset correction register, two's complement, internal *4 ;
28H	V_RMSOS	R/W	R	16	0	Voltage V RMS offset correction register, two's complement, internal *4 ;
29H	RMS_CREEP	R/W	R	12	0	RMS small signal threshold register, internal *4 ;
2AH	WA_LOS	R/W	R	twentyfour	0	Active small signal compensation register ;

						Higher 12 bits compensate B phase, complement code; Low 12 bits compensate phase A, complement code;
2BH	IA_CHOS	R/W	R	16	0	Current A channel bias adjustment register, two's complement
2CH	IB_CHOS	R/W	R	16	0	Current B channel bias adjustment register, two's complement
2DH	V_CHOS	R/W	R	16	0	Voltage V channel bias adjustment register, two's complement
2EH	IA_CHGN	R/W	R	16	0	Current A channel gain adjustment register, complement code
2FH	IB_CHGN	R/W	R	16	0	Current B channel gain adjustment register, two's complement
30H	V_CHGN	R/W	R	16	0	Voltage V channel gain adjustment register, two's complement
31H	LINECYC	R/W	R	12	000H	Line energy accumulation cycle number register
32H	ZXTOUT	R/W	R	16	FFFFH	Zero-Crossing Timeout Register
33H	SAGCYC	R/W	R	8	FFH	Drop Line Period Register
34H	SAGLVL	R/W	R	12	0	Dropout Voltage Threshold Register
35H	Reversed	R/W	R	twenty four	0	reserve
36H	I_PKLVL	R/W	R	twenty four	FFFFFFH	low 12 Bits [11:0] are current A, B peak threshold; The upper 12 bits [23:12] are reserved
37H	V_PKLVL	R/W	R	12	FFFH	Voltage V Peak Threshold Register
38H	AT_SEL	R/W	R	16	0	Output selection register, see "Output selection register" for details "Register" Description
39H	MASK	R/W	R	16	0	Interrupt mask register, see "Interrupt mask register" for details "Register" Description
3AH	STATUS	R	W	16	0	Interrupt status register, see "Interrupt Status Register" for details "Register" Description
special register						
3BH	READ	R	R	twenty four	0	Read data register. record the last read data

3CH	WRITE	R	R	twenty four	0	Write data register. record the last written data
3DH	CHKSUM	R	R	twenty four	015ABAH	Check register. For all writable calibration registers The numerical sum of
3EH	WRPROT	R/W	R	8	0	Write-protect setup register. When writing 55H, the table Indicates that write operations to writable registers are allowed.
3FH	SOFT_NRST	R/W	R	twenty four	0	When the input is 5A5A5AH, the system resets.

6.2 Instantaneous register description

Waveform registers (IA_WAVE, IB_WAVE, V_WAVE)

electric current A Wave register (IA_WAVE) Addr: 01H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
sign bit	IA_WAVE22	IA_WAVE21	IA_WAVE20…3	IA_WAVE2	IA_WAVE1	IA_WAVE0

electric current B Wave register (IB_WAVE) Addr: 02H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
sign bit	IB_WAVE22	IB_WAVE21	IB_WAVE20…3	IB_WAVE2	IB_WAVE1	IB_WAVE0

Voltage waveform register (V_WAVE) Addr： 03H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
sign bit	V_WAVE22	V_WAVE21	V_WAVE20…3	V_WAVE2	V_WAVE1	V_WAVE0

Notice:

The effective number of bits of the waveform register is 24 bits, Bit[23] is the sign bit, and the refresh rate is 14KHz.

Line Cycle Accumulated Active Energy Register（LINE_WATTHR）

Line energy accumulation active energy register (LINE_WATTHR) Addr： 04H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
L_AHR23	L_AHR22	L_AHR21	L_AHR20...3	L_AHR2	L_AHR1	L_AHR0

Notice:

This register accumulates（LINECYC + 1）× 0.02 second active power, and refreshes every（LINECYC + 1）× 0.02 second . Using the line cycle cumulative active energy mode can greatly simplify energy calibration and significantly reduce the time required to calibrate the meter. The accumulation time is set by the LINECYC register.

RMS registers（IA_RMS，IB_RMS，V_RMS）

electric current A effective value register (IA_RMS) Addr： 05H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

electric current B Effective value register (IB_RMS) Addr： 06H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

Voltage effective value register (V_RMS) Addr： 07H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
RMS23	RMS22	RMS21	RMS20…3	RMS2	RMS1	RMS0

Notice:

The RMS register is a 24-bit unsigned number, and the register refresh rate is 2.5Hz.

Power Factor Register（PF）

Power factor register (PF) Addr： 08H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PF23	PF22	PF21	PF20…3	PF2	PF1	PF0

Note: PF23 is the sign bit, complement code

If PF23=0,

If PF23=1,（（～）（～）（～）

(~)

Line Frequency /Period Register (FREQ)

Line Voltage /Frequency Periodizer (FREQ) Addr : 09H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PF23	PF22	PF21	PF20…3	PF2	PF1	PF0

Note: In the case of crystal oscillator 3.579545MHz , the measured frequency can also use the empirical formula: $f = \frac{87.3906 * fosc}{32 * FREQ}$;

fosc is crystal oscillator frequency;

Average active power registers（A_WATT，B_WATT）

Current A Channel Metering (A_WATT) Addr：0AH			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
sign bit	WATT22	WATT21	WATT20…3	WATT2	WATT1	WATT0

Current B Channel Metering (B_WATT) Addr：13H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
sign bit	WATT22	WATT21	WATT20…3	WATT2	WATT1	WATT0

Note: The average active power register is in 24-bit binary complement format, the highest bit is the sign bit, and the refresh rate is 2.5Hz. Its sign bit reflects the sign of the average power within 400mS.

Suppose the data in the average active power register is

WATT0 is used to calculate the _AP for: if WATT0<2^23,

AP=WATT0;

If WATT0>=2^23，AP = WATT0-2^24;

Assuming that the displayed active power is P and the conversion factor is Kp (when Kp is the rated active power input, the ratio of WATT0 reading to rated power), then:

P=AP/Kp;

Average Apparent Power Register（VA）

Average apparent power register (VA) Addr：0BH			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
VA23	VA22	VA21	VA20…3	VA2	VA1	VA0

Note: VA outputs the apparent power of the current metering channel according to the metering channel selected by the user; the coefficient when the apparent power is displayed is the same as the conversion coefficient Kp of active power.

Energy registers（WATTHR，VAHR，PWAHR，NWAHR）

Active energy register（WATTHR) Addr：0CH			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
WTTHR23	WATTHR22	WATTHR21	WATTHR20…3	WATTHR2	WATTHR1	WATTHR0

Apparent energy register（VAHR) Addr：0DH			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
VAHR23	VAHR 22	VAHR21	VAHR20…3	VAHR2	VAHR1	VAHR0

Positive active energy register (PWAHR) Addr：0EH	Type: read-only	Default value: 000000H

Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PWAHR23	PWAHR22	PWAHR21	PWAHR20…3	PWAHR2	PWAHR1	PWAHR0

Negative active energy register (NWAHR) Addr： 0FH			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
NWAHR23	NWAHR22	NWAHR21	NWAHR20…3	NWAHR2	NWAHR1	NWAHR0

Note: The energy register is not cleared after reading by default. The energy register can be set to be cleared after reading through the MODE register.

Transient Peak Registers（IA_PEAK，IB_PEAK，V_PEAK）

electric current A Transient Peak Register (IA_PEAK) Addr：10H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

electric current B Transient Peak Register (IB_PEAK) Addr：11H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

Voltage Transient Peak Register (V_PEAK) Addr：12H			Type: read-only		Default value: 000000H	
Bit23	Bit22	Bit21	20…3	Bit2	Bit1	Bit0
PEAK23	PEAK22	PEAK21	PEAK20…3	PEAK2	PEAK1	PEAK0

Note: The refresh rate of the transient peak register is 100Hz.

6.3 Calibration register

Operating Mode Register（MODE）

Working mode register (MODE) Addr：14H				Type: read and write		Default value: 000000H	
Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Location	the sign	Defaults	describe
0	WATT_SEL	0	Energy accumulation and CF output selection, the default is A-phase power, which is 1 When selecting B-phase power accumulation
1	AUTO_SEL	0	When MODE[1]=0, when it is detected that there is an unbalanced power consumption between phase A and phase B, it will not switch automatically. MODE[0] determines whether to measure by phase A or phase B; when MODE[1]=1, when A is detected Phase, B When there is an unbalanced power consumption between the phases, it will be switched automatically, and the one with the largest power consumption will be used for power

			measurement.
2	A_HPF_SEL	0	A aisle HPF select, use by default HPF, for 1 time bypass HPF
3	B_HPF_SEL	0	B channel HPF selection, HPF is used by default, HPF is bypassed when it is 1
4	V_HPF_SEL	0	V aisle HPF select, use by default HPF, for 1 time bypass HPF
5	COMP_SEL	0	Channel unbalance detection mode, the default is 0, use the current effective value of channel A and B to compare the unbalanced state of power consumption; when it is 1, use the power of phase A and phase B to compare the unbalanced state of power consumption; In the two comparison methods, the comparison threshold and channel switching methods are the same
6	ANTICREEP_SEL	0	Anti-creep mode selection, the default is 0, use the power threshold comparison method Type anti-submarine movement; when it is 1, turn on the timing anti-submarine mode;
7	SPI_MODE	0	reserve,
8, 9	CF_ADD_SEL	00	CF power accumulation method selection;

			Mode[9:8]=00; select CF output power absolute value energy;
			Mode[9:8]=01; Select CF to output positive energy;
			Mode[9:8]=10; Select CF output power algebra and energy;
			Mode[9:8]=11; Select CF to output negative energy;
10，11	FAULT_SEL	00	Two-phase unbalance comparison threshold setting，when the difference between the effective value of the sampling current of the live line and the neutral line or the difference between the active power of the A phase and the B phase exceeds the set threshold, the wrong power consumption indication signal is output FAULT
			Mode[11:10]=00; The judgment threshold for imbalance is 12.5%
			Mode[11:10]=01; The unbalanced judgment threshold is 6.25％；
			Mode[11:10]=10; The unbalanced judgment threshold is 3.125％；
			Mode[11:10]=11; The unbalanced judgment threshold is 10.16％；
12，13	INPUT_SEL	00	reserve
14,15	SPI_SEL	00	reserve
16	RMS_SETUP	0	RMS power-on stabilization time selection, the default is 400ms；it is 1 hour, Power-on stabilization time is 1.6 seconds;
17	CF_DISABLE	0	CF shutdown selection, the default is 0，CF works normally; when it is 1，The CF output is turned off, and the energy register stops accumulating;
18	LOS_ADJ	0	reserve
19	REVP_SEL	0	Reverse indication selection, when it is 0，select the sign bit of the 2.5Hz power register as the reverse indication, WA_CREEP is valid; when it is 1，select the real-time power sign bit as the reverse indication, REVP_CREEP Valid; only affects STATUS[6] flags;

20	ENG_REG_CLR	0	set to 1, all energy registers are automatically cleared after a read operation Zero; when set to 0, all energy registers will not be automatically cleared after the read operation, but will only continue to accumulate automatically;
twenty one	WATTHR_SEL	0	Active energy register accumulation method selection, choose 0 as default, Number and accumulation; when 1 is selected, it is absolute value accumulation;
23~22	Reversed	0	reserve

Gain Register (GAIN)

Gain register (GAIN) Addr: 15H		Type: read and write	Default value: 000H
Bit11 ~ 8	Bit7 ~ 4	Bit3 ~ 0	
Voltage channel PGA gain selection	Current B channel PGA gain selection	Current A channel PGA gain selection	

Take A channel PGA gain selection as an example, use [3:0] bits to adjust:

X000 1 Multiplier

X001 2 Multiplier

X010 4 Multiplier

X011 8 Multiplier

X100 16 Multiplier

X101 24 Multiplier

X110 32 Multiplier

X111 cannot be set

Unbalance Mask Threshold Register (FAULTLVL)

Unbalance shielding threshold (FAULTLVL) Addr : 16H	Type: read and write	Default value: 044H
Bit11 ~ 8	Bit7 ~ 4	Bit3 ~ 0

It is used to set the threshold of whether the Fault detection function works when the dual-channel is unbalanced; the dual-channel unbalanced judgment can be based on the effective value or power comparison (set in the working mode MODE register)

FAULTLVL=RMS_Reg/256 or FAULTLVL=WATT_Reg/256

Anti-Creep Power Threshold Register (WA_CREEP)

Anti-creep power threshold (WA_CREEP) Addr : 17H	Type: read and write	Default: FFF02BH
Bit23~12	Bit11~0	
Anti-creep time threshold WA_CREEP_H	Anti-creep power threshold WA_CREEP_L	

Bit11 ~ 0 are used to set the anti-creep active power threshold. When the instantaneous active power is lower than the anti-creep power threshold, the instantaneous active power is cut to 0 and does not participate in active energy accumulation. Correspondence between setting value and average active power register: WA_CREEP_L=WATT_Reg/(2*1.3655)

Bit23 ~ 12 are used to set the anti-creep time threshold, 1LSB=4.6 seconds, need to enable timing anti-creep in the working mode register MODE setting.

Reverse Indication Threshold Register (WA_REVP)

Reverse indication threshold (WA_REVP) Addr : 18H	Type: read and write	Default value: 087H
Bit11 ~ 8	Bit7 ~ 4	Bit3 ~ 0

12 Bit unsigned number, when the input active power signal is negative and the absolute value is less than this threshold, REVP in the interrupt status register The indication bit is not refreshed, and is set to 0, so that under no-load conditions, even if there is a small noise signal, REVP interrupt will not be generated . Correspondence between setting value and average active power register: WA_REVP=WATT_Reg/(32*1.3655)

Active CF Scaling Register (WA_CFDIV)

meritorious service CF Zoom ratio (WA_CFDIV) Addr : 19H	Type: read and write	Default value: 001H
Bit11 ~ 8	Bit7 ~ 4	Bit3 ~ 0

Adjust the output frequency of CF.

Current voltage channel ±660mV peak-to-peak (467mV rms) input				
WA_CFDIV	CF frequency (Hz)	active power	IA_RMS	V_RMS
1(0x01)	1.95	6500000	5650000	5650000

2(0x02)	3.91			
4(0x04)	7.81			
8(0x08)	15.63			
16(0x10)	31.25			
32(0x20)	62.50			
64(0x40)	125.00			
128(0x80)	250.00			
256(0x100)	500.00			

Active Power Offset Calibration Registers (A_WATTOS, B_WATTOS)

A channel active power offset calibration (A_WATTOS) Addr： 1AH		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

B channel active power offset calibration (B_WATTOS) Addr： 1BH		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

Complement code, used to adjust the active power deviation in the case of small signal;

For example, in the case of a small signal, the data of the active power register X_WATT is WATT_Data , and the active power error is Err , then the value of the active power offset calibration register is:

int(WATT_Data*(-Err)/1.3655)*8 if Err<0;

int(WATT_Data*(-Err)/1.3655)*8+65536 if Err>=0;

active power gain adjustment register

(A_WATTGN, B_WATTGN)

A channel active power gain adjustment (A_WATTGN) Addr： 1CH		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

B channel active power gain adjustment (B_WATTGN) Addr： 1DH		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

Complement code, used to adjust the scaling ratio of active power, the adjustment range is ± 50%

$$\mathrm{WATT\_Reg} = \mathit{Active\ Power} \times (1 + \frac{X\_WATTWG}{2^{16}}) \quad --$$

BG_CTRL register (BG_CTRL)

Analog circuit control (BG_CTRL) Addr： 1FH		Type: read and write	Default value: 0FA3H
Bit21 ～ 16	Bit15 ～ 8	Bit7 ~ 4	Bit3 ~ 0

Bit[21:16]

Bit[15:0]

Phase Correction Register (PHCAL)

Phase correction (PHCAL) Addr： 20H				Type: read and write		Default value: 000000H	
enable bit	Adjust bit						
D7	D6	D5	D4	D3	D2	D1	D0
Current A channel phase correction							

enable bit	Adjust bit						
D15	D14	D13	D12	D11	D10	D9	D8
Current B channel phase correction							
enable bit	Adjust bit						
D23	D22	D21	D20	D19	D18	D17	D16
Voltage Channel Phase Correction							

The principle of phase compensation is to introduce a small time delay into the signal processing circuit to compensate for small phase errors;

D7 is the enable bit. When =1, phase compensation is turned on, and when =0, phase compensation is turned off;

D5...D0 is the delay or advance time, 0.5587us/1LSB. The corresponding resolution is 0.01, the maximum αδφυσταβλε ισ 0.635. Tested under 100% Un, standard current Ib 0.5L, measured error Err,

$$\theta \approx \arcsin(\frac{|Err|}{1.732})$$

register value = (int(θ / 0.01) + 127 ; int It is a rounding operation; (It is recommended to round off the decimal part to improve the adjustment accuracy)

If Err is positive, change the phase of the current channel; if Err is negative, change the phase of the voltage channel;

Apparent Power Offset Calibration Register (VA_OS)

Apparent Power Offset Calibration (VAOS) Addr: 21H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ~ 8	Bit7 ~ 4	Bit3 ~ 0

It is a 16-bit register, the default value is 0000H, expressed in 2's complement form. VAOS is used to eliminate the bias in the calculation of apparent power . Offset correction can bring the value in the apparent power register close to 0 at no load .

$$VA = VA_0 + VAOS*1.3655/8$$

Apparent power gain adjustment register (VAGN)

Apparent power gain adjustment (VAGN) Addr: 22H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ~ 8	Bit7 ~ 4	Bit3 ~ 0

16-bit signed number, the default value is 0000H. The gain of apparent power is adjusted with the data in 2's complement form, and the adjustable range is ± 50%.

$$output \quad VA = VA_0 \times (1 + \frac{VAGN}{2^{16}})$$

RMS gain adjustment registers (IA_RMSGN, IB_RMSGN, V_RMSGN)

Current A RMS Gain Adjustment (IA_RMSGN) Addr: 23H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ~ 8	Bit7 ~ 4	Bit3 ~ 0

Current B RMS gain adjustment (IB_RMSGN) Addr: 24H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ~ 8	Bit7 ~ 4	Bit3 ~ 0

Voltage RMS gain adjustment (V_RMSGN) Addr：25H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

16-bit signed number, its default value is 0000H. , respectively adjust the current A channel and the current B channel with the data in the form of 2's complement channel and the rms gain of the voltage Vchannel.

$$output\ RMS = {}_{0} \times (1 + \frac{X\_RMSGN}{2^{16}})$$

RMS Offset Correction Registers (IA_RMSOS, IB_RMSOS, V_RMSOS)

Current A RMS Offset Correction (IA_RMSOS) Addr： 26H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

Current B RMS Offset Correction (IB_RMSOS) Addr：27H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ~ 8	Bit7 ~ 4	Bit3 ~ 0

Voltage RMS offset correction (V_RMSOS) Addr：28H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ~ 8	Bit7 ~ 4	Bit3 ~ 0

16-bit registers. They use the data in the form of 2's complement to eliminate the deviation in the effective value calculation of the current A channel, the current B channel and the voltage V channel respectively. This deviation may come from input noise, since there is a squaring step in calculating the rms value , which may introduce a dc offset due to noise. Offset correction can make the value in the rms register close to 0 at no load .

$$I_{ARMS} = \sqrt{I_{ARMS0}^{2} + IA\_RMSOS \times 2^{13}}$$

RMS Small Signal Threshold Register (RMS_CREEP)

RMS small signal threshold (RMS_CREEP) Addr：29H		Type: read and write	Default value: 000H
Bit11	Bit10 ~ 8	Bit7 ~ 4	Bit3 ~ 0

If the effective value is smaller than the setting value of the effective value small signal threshold register, the RMS register value is 0；

Correspondence between RMS_CREEP register and X_RMS register

$$RMS = \begin{cases} 0 & RMS\_RMS\_CREEP / (1.3655 * 2) \\ PM\Sigma, & RMS >= RMS\_CREEP / (1.3655 * 2) \end{cases}$$

Active Small Signal Compensation Register (WA_LOS)

Active small signal compensation (WA_LOS) Addr：2AH		Type: read and write	Default value: 0000H
Bit23 (sign bit)	Bit22 ~ 12	Bit11 (sign bit)	Bit10 ~ 0
B channel active power		A channel active power	

24-bit register compensates the active power error when inputting small signals with data in 2's complement form. High 12 bits compensate B channel power, low 12 bits compensate A channel power

$$Active\ Power = ActivePower_{0} + \text{WATTOS}*1.3655$$

Channel Offset Adjustment Registers (IA_CHOS, IB_CHOS, V_CHOS)

reserve

Channel gain adjustment registers (IA_CHGN, IB_CHGN, V_CHGN)

electric current A Channel gain adjustment (IA_CHGN) Addr : 2EH		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

electric current B Channel gain adjustment (IB_CHGN) Addr : 2FH		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

Voltage channel gain adjustment (V_CHGN) Addr : 30H		Type: read and write	Default value: 0000H
Bit15 (sign bit)	Bit14 ～ 8	Bit7 ~ 4	Bit3 ~ 0

16-bit signed number, the default value is 0000H. They adjust the gain of the current A channel, current B channel and voltage V channel with data in 2's complement form, and the adjustable range is ± 50%.

$$output\ \ WAVE = WAVE \times (1 + \frac{X\_CHGN}{2^{15}})$$

For example: write 7FFFH (hexadecimal) to IA_CHGN, the output waveform amplitude increases by 50%, because 7FFFH = 32767 (decimal), 32767 / 65535 = 0.5. Similarly, write 8001H When, the amplitude of the output waveform decreases 50%.

Line cycle accumulation cycle number register (LINECYC)

Line cycle accumulation cycle number (LINECYC) Addr: 31H			Type: read and write		Default value: 000H
D11	D10	D9	D8…D2	D1	D0

Set the cumulative time of line cycle cumulative active energy register (LINE_WATTHR 04H). 1LSB=20mS;

Cumulative cycle time =(LINE CYC + 1)* 0.02 seconds, line cycle accumulated active energy register (LINE_WATTHR04H) Refresh every (LINECYC +1) *0.02 seconds; the value is the active energy accumulation of the previous (LINECYC+1) *0.02 seconds.

Zero-crossing time-out register (ZXTOUT)

Zero- cross timeout (ZXTOUT) Addr: 32H		Type: read and write	Default value: FFFFH
Bit15 ~ 12	Bit11 ~ 8	Bit7 ~ 4	Bit3 ~ 0

The resolution of this register is 70.5us/LSB.

Fall Line Cycle Register (SAGCYC)

Falling line cycle (SAGCYC) Addr: 33H				Type: read and write		Default value: FFH	
D7	D6	D5	D4	D3	D2	D1	D0

The resolution of this register is 10ms/LSB.

Drop Voltage Threshold Register (SAGLVL)

Drop voltage threshold (SAGLVL) Addr: 34H		Type: read and write	Default value: 000H
Bit11	Bit10 ~ 8	Bit7 ~ 4	Bit3 ~ 0

The register value is compared with the voltage effective value register V_RMS/2798.

Peak Threshold Register (I_PKLVL, V_PKLVL)

Current peak threshold (I_PKLVL) Addr: 36H		Type: read and write	Default value: 000000H
Bit23 ~ Bit16	Bit15 ~ 12	Bit11 ~ 4	Bit3 ~ 0
reserve		Current A, B peak threshold	

Voltage peak threshold (V_PKLVL) Addr： 37H		Type: read and write	Default value: 000H
Bit11	Bit10 ～ 8	Bit7 ~ 4	Bit3 ~ 0

Peak threshold register value = corresponding effective value register value /2798.

Output Select Register (AT_SEL)

Output selection (AT_SEL) Addr： 38H		Type: read and write	Default value: 0000H
Bit15 ～ 12	Bit11 ~ 8	Bit7 ~ 4	Bit3 ~ 0
AT3	AT2	reserve	reserve

No corresponding pin; this function is invalid;

Interrupt Mask Register (MASK)

Interrupt mask (MASK) Addr： 39H			Type: read and write	Default value: 0000H	
D15	D14	D13	D12…D2	D1	D0

the corresponding position is 1, the corresponding function has IRQ output. No corresponding pin; this function is invalid;

Interrupt Status Register (STATUS)

Interrupt status (STATUS) Addr: 3AH			Type: read and write	Default value: 0000H	
D15	D14	D13	D12…D2	D1	D0

Location	interrupt flag	Defaults	describe
0	SAG	0	Indicates a line dip interrupt
1	ZXTO	0	Indicates that a zero-crossing timeout interrupt is generated
2	ZX	0	Indicates the generated voltage waveform sign bit
3	PKIA	0	Indicate current A RMS peak value exceeds I_PKLVL interrupt
4	PKIB	0	Indicate current B RMS peak value exceeds I_PKLVL interrupt
5	PKV	0	Indicates that the voltage RMS peak value exceeds V_PKLVL interrupt
6	REVP	0	Indicates a sign change in the active power calculation
7	APEHF	0	Indicates that bit 23 of the WATTHR register [23:0] goes to 1 (half Full)
8	VAPEHF	0	Instruct VAHR Bit 23 of register [23:0] becomes 1 (half full)
9	FAULT	0	Indicates that the two channels of current AB are unbalanced
10	CHSEL	0	Indicates the measurement channel, 0 is the current A channel, 1 is the current B aisle
11	VREF_LOW	0	Indicates that the reference voltage value is low, when it is 1, VREF<2V; when it is 0 normal
12	SPI_DIN_ERR	0	reserve
13	UART_DIN_ERR	0	Instruct UART Write error status flag, 1 Exceptions are written when, Writing is normal when it is 0
14	VREF_HIGH	0	that the reference voltage value is too high. When it is 1, VREF>2.9V; Normal at 0
15	Reversed	0	

Check register (CHKSUM)

Check (CHKSUM) Addr： 3DH				Type: read and write	Default: 015ABAH
D23	D22	D21	D20…D2	D1	D0

Sum the values of all writable registers, from 14H to 39H (35H does not participate in the checksum), take the lower 24 bits.

Write Protection Setting Register (WRPROT)

Write protection setting (WRPROT) Addr： 3EH				Type: read and write		Default value: 00H	
D7	D6	D5	D4	D3	D2	D1	D0

It is used to protect the registers that can be written through SPI . Writing 55H means that the write operation to the writable register is allowed. When writing other values, the write operation is prohibited.

Soft reset setting （ SOFT_NRST）

Soft reset (SOFT_NRST) Addr： 3FH			type: write		Default value: 00H	
D23	D22	D21	……	D2	D1	D0

can be issued through the UART interface to control the BL6523G system reset. The logic sequence of the reset operation is as follows:

1）Open the write protection, write 55H to the WRPROT（ 3EH ）register ;

2）Soft reset instruction, SOFT_NRST（ 3FH ）register writes 5A5A5AH ;

3）waiting time t After the chip is reset to the initial state, subsequent operations can be performed. Delay time 300uS.

Note: The above specification changes due to process or design changes will not be notified separately. Please feel free to request the latest version of the product specification.