RS-485 Transceiver with Polarity Adaptive

product description

BL3085N is a 5V power supply, half-duplex, adaptive bus polarity RS-485 transceiver, the chip contains a driver and a receiver. BL3085N integrates the bus polarity correction circuit, and the polarity discrimination time is 80ms . In the communication system composed of RS-485 communication chip , it can automatically adapt to the polarity of the bus port.

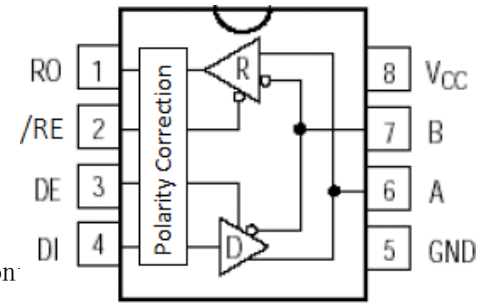
The BL3085N uses a slew-rate-limited driver, which can significantly reduce EMI and reflections caused by improperly terminated cables, enabling error-free data transmission up to 500kbps . BL3085N has a built-in fail-safe circuit to ensure that the output of the receiver is in a logic high state when the input of the receiver is open or short-circuited.

BL3085N receiver is 1/8 unit load, allowing up to 256 transceivers to be connected to the bus to realize half-duplex communication. BL3085N I/O pins have ± 15kV IEC 61000-4-2 contact discharge protection capability.

Product Features

- +5V working voltage
- Adaptive Bus Polarity
- Polarity discrimination time 80ms
- Built-in fail-safe circuit
- Up to 500kbps transfer rate
- Bus allows up to 256 transceivers
- I/O pin ESD protection: ± 15kV IEC 61000-4-2 , con
- SOP8 package

Block Diagram



Application field

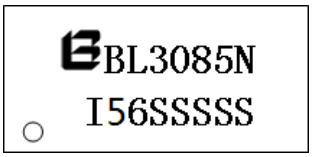
- smart meter
- Collection terminal
- industrial control
- security monitor

Note: The chip version ″ I56 ″ is determined by the first three digits in the second row of the chip silkscreen

Ordering information

型号	封装	丝印
BL3085N(I56)	SOP8	BL3085N I56SSSSS

silk screen information



Among them: "I56" is the chip version number

" SSSSS " represents the 4th to 8th digits of the card number

Pin definition

serial number	name	function
1	RO	receiver output
2	/RE	Receiver output enable. RO output is valid when / RE is low ; RO is high-impedance when / RE is high
3	DE	Driver output enable. The driver output is valid when DE is high level, and the output is high impedance state when DE is low level
4	DI	drive input
5	GND	grounding
6	A	Receiver non-inverting input and driver non-inverting output by default
7	B	Receiver inverting input and driver inverting output by default
8	V_{CC}	power supply

Driver Truth Table

enter			output	
/RE	DE	DI	A	B
Positive state				
x	1	1	1	0

x	1	0	0	1
0	0	x	High-Z	High-Z
1	0	x	Shutdown（ High-Z ）	
Reverse state				
x	1	1	0	1
x	1	0	1	0

0	0	x	High-Z	High-Z
1	0	x	Shutdown（ High-Z ）	

Receiver Truth Table

enter			output
/RE	DE	AB	RO
0	x	>100mV	1
0	x	<-100mV	The polarity judgment time is 0 1 outside the polarity judgment time
0	x	open / short	1 (outside the polarity judgment time)
1	1	x	High-Z
1	0	x	Shutdown（ High-Z ）

Limit parameter

parameters	the symbol	limit value	unit
Operating Voltage	V_{CC}	+7	V
Control input voltage	/RE, DE	-0.3 to V_{CC} +0.3	V
Driver input voltage	DI	-0.3 to V_{CC} +0.3	V
Driver output voltage	A, B	±13	V
Receiver input voltage	A, B	±13	V
Receiver output voltage	RO	-0.3 to V_{CC} +0.3	V

temperature range

Specified service temperature	-40~+85 ℃
Limit temperature	-55~+125 ℃
storage temperature	-65~+150 ℃

DC Electrical Characteristics

（ V CC =+ 5 V±5%, TA = -40 ℃ ~ + 85 ℃ ， typical value at VCC = + 5 V， TA = 25 ℃ ）(Note 1)

parameter	symbol	Test Conditions	minimum value	typical value	maximum value	unit
Operating Voltage	V_{CC}		4.5		5.5	V
driver						
Differential driver output (no load)	V_{OD1}	Figure 1			V_{CC}	V
Differential Driver Output	V_{OD2}	Figure 1， R=27Ω	1.5			V
The magnitude of the differential output voltage Variation (Note 2)	ΔV_{OD}	Figure 1， R=27Ω			0.2	V
Driver Common Mode Output Voltage	$VOC\_$	Figure 1， R=27Ω	1.0		3.0	V
Amplitude variation of common mode voltage (Note 2)	ΔV_{OC}	Figure 1， R=27Ω			0.2	V
input high voltage	$V\_$	DE,DI,/RE	2.0			V
input low voltage	$VIL\_$	DE,DI,/RE			0.8	V
DI input hysteresis	V_{HYS}			100		mV
Input Current (A, B)	I_{IN4}	DE=GND V_{CC} =GND or 5.25V; V_{IN} =12V			125	μA
		DE=GND V_{CC} =GND or 5.25V; V_{IN} =-7V	-75			
Driver short circuit output current	I_{OSD}	A Pin Short to B Pin	-100		100	mA
receiver						
Receiver Differential Threshold Voltage	$VTH\_$	-7V ≤ VCM ≤ 12V _	-100		100	mV
Receiver Input Hysteresis	△ V_{TH}			40		mV
Receiver output high voltage	V_{OH}	I_O =-8mA, V_{ID} =200mV	4.0			V
Receiver output	V_{OL}	I_O =8mA,V_{ID} =-			0.4	V

low voltage		200mV					
Receiver Tri-State Output Current	QU R _					±1	μA
Receiver input impedance	R_{IN}	-7V ≤ VCM ≤ 12V _		96			KΩ
Receiver output short circuit current	OSR _	0V ≤ V_{RO} ≤ V_{CC}		±7		±95	mA
supply current							
supply current	I_{CC}	No load , /RE=DI=GND or V_{CC}	DE=V_{CC}		350	600	μA
			DE=GND		370	600	μA
Standby Mode Supply Current	I_{SHDN}	DE=GND, /RE= VCC , DI=V_{CC} or GND				10	μA
polarity discrimination time	T_{DTECT}				80		ms

Note 1: All currents into the device are positive and all currents out of the device are negative; all voltages are to ground unless otherwise specified. Note 2: When DI input changes state, △ V_{OD} and △ V_{OC} V_{OD} _ and V_{OC} amount of change.

transmission characteristics

（ VCC=+5V±5%, TA=-40 ℃ ~ +85 ℃ , the typical value is VCC=+5V , TA = 25 ℃ ）

parameter	symbol	condition	minimum value	typical value	maximum value	unit
Driver input to output delay	T_{DPLH}	Figures 3 and 5 , R_{DIFF} =54Ω C_{L1} =C_{L2} =100pF		300	800	ns
	T_{DPHL}			300	800	
Driver output delay difference $\|T_{DPLH} - T_{DPHL}\|$	T_{DSKEW}	Figures 3 and 5 , R_{DIFF} =54Ω C_{L1} =C_{L2} =100pF			100	ns
Driver Rise or Fall Time	T_{DR} , T_{DF}	Figures 3 and 5 , R_{DIFF} =54Ω C_{L1} =C_{L2} =100pF		420	900	ns
maximum rate	F_{MAX}		500			Kbps
Driver Enable to Output High	TZH _	Figures 4 and 6 , C_L =100pF S2 Closed			300	ns
Driver Enable to Input low level	QZL _	Figures 4 and 6 , C_L =100pF S1 Closed			500	ns
drives the output low from the to off time	DLZ _	Figures 4 and 6 , C_L =15pF S1 Closed			900	ns
drives the output high from the to off time	T_{DHZ}	Figures 4 and 6 , C_L =15pF S2 Closed			800	ns
Receiver input and output delay	T_{RPLH} RPHL _	7 and 9 , _ ; rise and fall time of VID ≦ 15ns		150	300	ns
$\|T_{RPLH} - T_{RPHL}\|$ Difference between receiver input and output delay	T_{RSKD}	7 and 9 , _ ; rise and fall time of VID ≦ 15ns		10		ns

Receiver Enable to Input out low	QUR_{-}	Figures 2 and 8, C_{RL} =15pF S1 Closed		20	50	ns
Receiver Enable to Input high	QUR_{-}	Figures 2 and 8, C_{RL} =15pF S2 Closed		20	50	ns
receiver outputs low from the to shutdown	RLZ_{-}	Figures 2 and 8, C_{RL} =15pF S1 Closed		30	60	ns
Receiver output high from to shutdown	T_R	Figures 2 and 8, C_{RL} =15pF S2 Closed		30	60	ns
circuit off time	T_{SHDN}			500	1000	ns
Driver Enable from Standby to Output High	$T_{DZH(SHDN)}$	Figures 4 and 6, C_L =100pF S2 Closed			2500	ns

from standby to output low driver enable	$T_{DZL(SHDN)}$	Figures 4 and 6, C_L =100pF S1 Closed			2500	ns
Receiver Enable from Standby to Output High	$T_{RZH (SHDN)}$	Figures 2 and 8, C_{RL} =15pF S2 Closed			2500	ns
Receiver Enable from Standby to Output Low	$T_{RZL (SHDN)}$	Figures 2 and 8, C_{RL} =15pF S1 Closed			2500	NS

test circuit

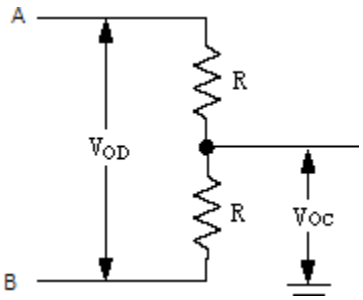


Figure 1： Driver DC Test Load

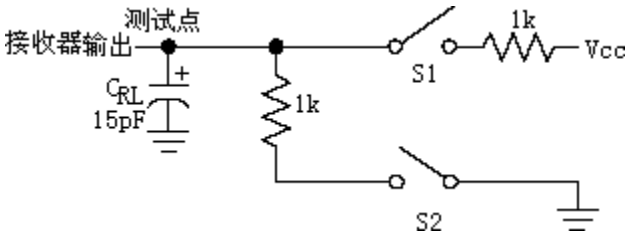


Figure 2： Receiver Enable/Disable Timing Test load

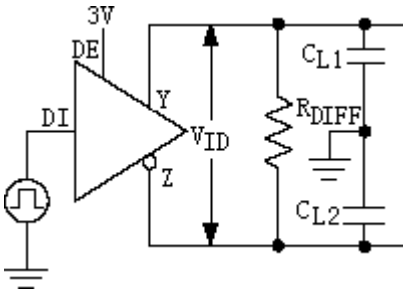


图 3：Driver Timing Test Circuit

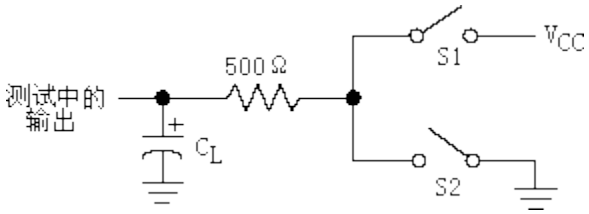


图 4：Driver Enable/Disable Timing Test Load

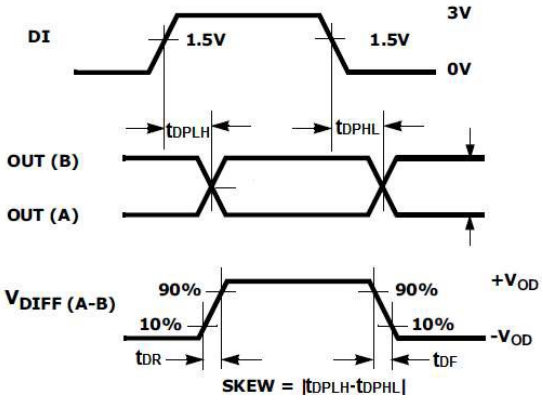


图 5：Driver Propagation Delays

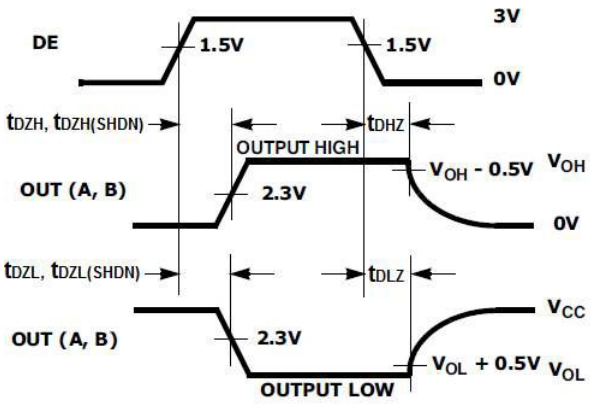


图 6：Driver Enable and Disable Times

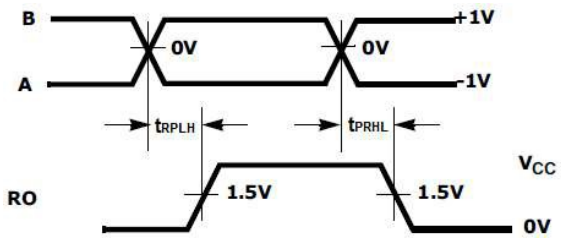


Figure 7： Receiver Propagation Delays

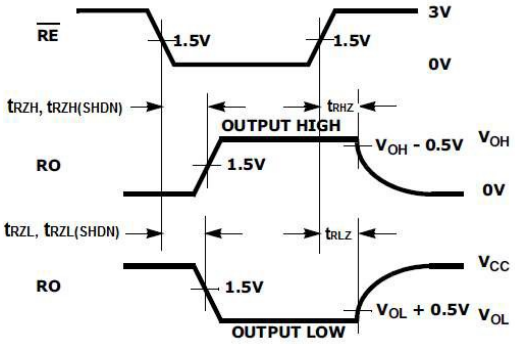


Figure 8： Receiver Enable and Disable Times

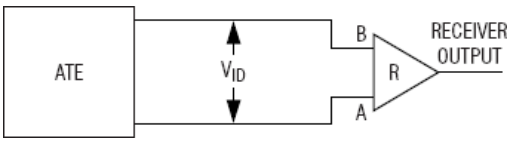


Figure 9： Receiver Propagation Delay Test Circuit

Polarity adaptive function

In the RS-485 communication network, the RS-485 transceiver as the host terminal (such as a concentrator) is connected to the RS -485 transceiver as a slave terminal (such as a smart meter) through two buses . In a traditional RS-485 system, the polarity of the two buses needs to be distinguished, and the polarities of all RS-485 transceiver bus ports in the system need to match. BL3085N has a built-in polarity correction circuit, which can automatically detect the bus polarity of the system after power-on, and automatically adjust the polarity of the port to match the polarity of the system bus after 80ms.

BL3085N on the slave side requires the cooperation of the master side. In order to judge the bus polarity, the following conditions must be met: 1. The master side needs to define the bus polarity by designing appropriate pull-up and pull-down resistors on the A and B ports.

2. The A and B ports of the slave BL3085N cannot be designed with pull-up resistors and pull-down resistors.

3. The slave terminal must be in the receiving state during the polarity discrimination time.

4. The bus must be idle within the polarity discrimination time.

After the polarity discrimination time elapses, the polarity correction is completed. The state of the bus polarity is latched within the transceiver and maintained for subsequent data transfers. A continuous ″ 0 ″ or ″ 1 ″ data string lasting longer than the polarity discrimination time may accidentally trigger a wrong polarity correction and must be avoided. Figure 10 shows a typical network application circuit.

Typical Application Diagram

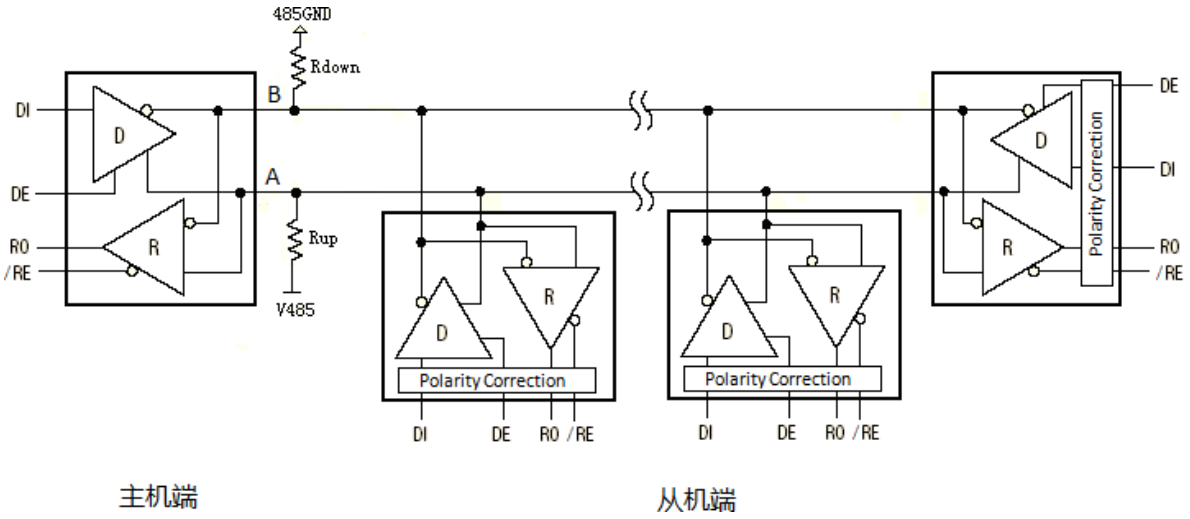
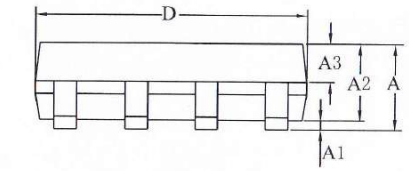
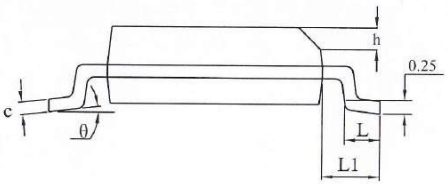
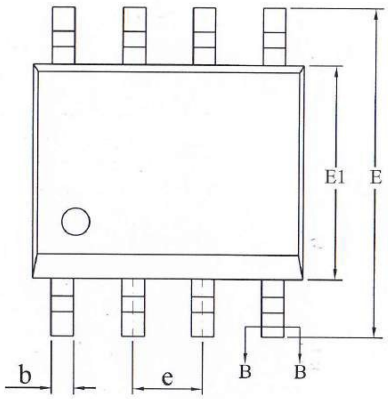


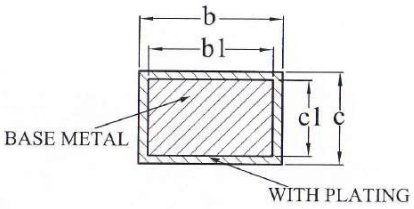
Figure 10：Non-polar RS-485 network application diagram

Package size (SOP8)









SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	—	0.48
b1	0.38	0.41	0.44
c	0.20	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°