RS-485 Transceiver with Fail -Safe

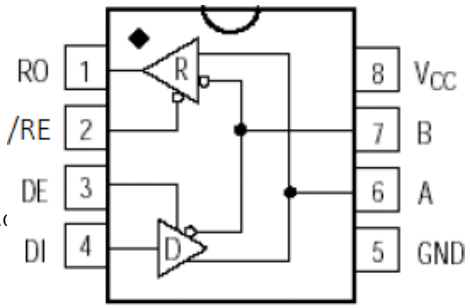
product description

BL1587 is a half-duplex RS-485 transceiver, the chip contains a driver and a receiver. BL1587 can provide the highest transfer rate of 2Mbps . The chip has a built-in fail-safe circuit to ensure that the output of the receiver is in a logic high state when the input of the receiver is open or short-circuited . The BL1587 has a 1/4 unit load receiver input impedance, allowing up to 128 transceivers on the bus .

Product Features

- +5V working voltage
- Maximum transfer rate: 2Mbps
- Built-in fail-safe circuit
- Bus allows up to 128 transceivers
- I/O pin ESD protection: ± 15kV IEC 61000-4-2 , contac
- SOP8 package

Block Diagram



Application field

- smart meter
- industrial control
- security monitor

Pin definition

serial number	name	function
1	RO	receiver output
2	/RE	Receiver output enable. RO output is valid when /RE is low level; RO is high impedance state when /RE is high level
3	DE	Driver output enable. The driver output is valid when DE is high level, and the output is high impedance state when DE is low level
4	DI	drive input
5	GND	grounding
6	A	Receiver non-inverting input and driver non-inverting output
7	B	Receiver inverting input and driver inverting output
8	V_{CC}	power supply

Driver Truth Table

enter			output	
/RE	DE	DI	A	B
x	1	1	1	0
x	1	0	0	1
0	0	x	High-Z	High-Z
1	0	x	Shutdown（ High-Z ）	

Receiver Truth Table

enter			output
/RE	DE	AB	RO
0	x	>-50mV	1

0	x	<-200mV	0
0	x	open / short	1
1	1	x	High-Z
1	0	x	Shutdown（ High-Z ）

Limit parameter

parameters	the symbol	limit value	unit
Operating Voltage	V_{CC}	+7	V
Control input voltage	/RE, DE	-0.3 to V_{CC}+0.3	V
Driver input voltage	DI	-0.3 to V_{CC}+0.3	V
Driver output voltage	A, B	±13	V
Receiver input voltage	A, B	±13	V
Receiver output voltage	RO	-0.3 to V_{CC}+0.3	V
range of working temperature		-40~+85	℃

DC Electrical Characteristics

（VCC=+5V ± 5%，TA=-40℃～ +85℃, typical value is at VCC=+5V, TA = 25℃)(Note 1)

parameter	symbol	Test Conditions	minimum value	typical value	maximum value	unit
Operating Voltage	V_{CC}		4.5		5.5	V
driver						
Differential driver output (no load)	V_{OD1}	Figure 1			V_{CC}	V
Differential Driver Output	V_{OD2}	VCC=5V Figure 1, R=27Ω	1.5	2.1		V
The magnitude of the differential output voltage Variation (Note 2)	ΔV_{OD}	Figure 1, R=27Ω			0.2	V
Driver Common Mode Output Voltage	VOC_	Figure 1, R=27Ω	1.0		3.0	V
Amplitude variation of common mode voltage (Note 2)	ΔV_{OC}	Figure 1, R=27Ω			0.2	V
input high voltage	V_	DE,DI,/RE	2.0			V

input low voltage	VIL	DE,DI,/RE				0.8	V
DI input hysteresis	V_{HYS}				100		mV
Input Current（A，B）	I_{IN4}	DE=GND V_{CC} =GND or 5.25V	V_{IN} =12V			220	μA
			V_{IN} =-7V	-120			
Driver short circuit output current	I_{OSD}	A Pin Short to B Pin		-100		100	mA
receiver							
Receiver Differential Threshold Voltage	VTH_	-7V ≤ VCM ≤ 12V		-200	-125	-50	mV

Receiver Input Hysteresis	△ V_{TH}			40		mV
Receiver output high voltage	V_{OH}	I_O=-8mA, V_{ID}=-50mV	4.0			V
Receiver output low voltage	V_{OL}	I_O=8mA,V_{ID}=-200mV			0.4	V
Receiver Tri-State Output Current	QUR_				±1	μA
Receiver input impedance	R_{IN}	-7V ≤ VCM ≤ 12V_	48			KΩ
Receiver output short circuit current	OSR_	0V ≤ V_{RO} ≤ V_{CC}	±7		±95	mA
supply current						
supply current	I_{CC}	No load , /RE=DI= GND or V_{CC} DE=V_{CC}		900		μA
		DE=GND		900		μA
Standby Mode Supply Current	I_{SHDN}	DE=GND, /RE= V_{CC} , DI=V_{CC} or GND			10	μA

Note 1：All currents into the device are positive and all currents out of the device are negative; all voltages are to ground unless otherwise specified. Note 2：When DI input changes state, △ V_{OD} and △ V_{OC} V_{OD}_ and V_{OC} amount of change.

transmission characteristics

（VCC=+5V±5%, TA=-40℃ ~ +85℃，the typical value is VCC=+5V，TA＝25℃）

parameter	symbol	condition	minimum value	typical value	maximum value	unit
Driver input to output delay	wxya_	Figures 3 and 5， R_{DIFF} =54Ω C_{L1}=C_{L2}=100pF		13		ns
	t_{DPHL}			17		
Driver output delay difference |T_{DPLH} − T_{DPHL}|	tDSKEW_	Figures 3 and 5， R_{DIFF} =54Ω C_{L1}=C_{L2}=100pF		5		ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 3 and 5， R_{DIFF} =54Ω C_{L1}=C_{L2}=100pF		8		ns
maximum rate	F_{MAX}		2			Mbps

Driver Enable to Output High	wxya _	Figure 4 6 , C_L=100pF S2 and Closed		20		ns
Driver Enable to Input low level	wxya _	Figure 4 6 , C_L=100pF S1 and Closed		28		ns
drives the output low from the to off time	lm w	Figure 4 6 , C_L=15pF S1 and Closed		19		ns
drives the output high from the to off time	wxya _	Figure 4 6 , C_L=15pF S2 and Closed		16		ns
Receiver input and output Delay	t_{RPLH} tRPHL _	7 and 9 , _		42		ns

		; rise and fall time of VID ≦ 15ns				
$\|T_{RPLH} - T_{RPHL}\|$ Difference between receiver input and output delay	t_{RSKD}	7 and 9, _ ; rise and fall time of VID ≦ 15ns		5		ns
Receiver Enable to Input out low	wxya _	Figure 2 8, C_{RL}=15pF S1 and Closed		10		ns
Receiver Enable to Input high	wxya _	Figure 2 8, C_{RL}=15pF S2 and Closed		45		ns
receiver outputs low from the to shutdown	lm_w	Figure 2 8, C_{RL}=15pF S1 and Closed		10		ns
Receiver output high from to shutdown	wxya _	Figure 2 8, C_{RL}=15pF S2 and Closed		45		ns
circuit off time	t_{SHDN}			100		ns
Driver Enable from Standby to Output High	$t_{DZH(SHDN)}$	Figures 4 and 6, C_L =100pF S2 Closed		1600		ns
from standby to output low driver enable	$t_{DZL(SHDN)}$	Figure 4 6, C_L=100pF S1 and Closed		1600		ns
Receiver Enable from Standby to Output High	$t_{RZH(SHDN)}$	Figure 2 8, C_{RL}=15pF S2 and Closed		1500		ns
Receiver Enable from Standby to Output Low	$t_{RZL(SHDN)}$	Figure 2 8, C_{RL}=15pF S1 and Closed		2300		ns

test circuit

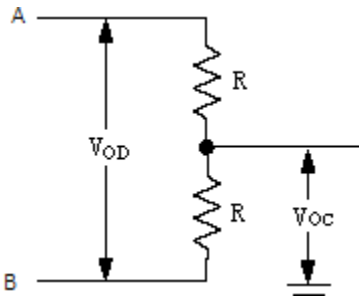


Figure 1： Driver DC Test Load

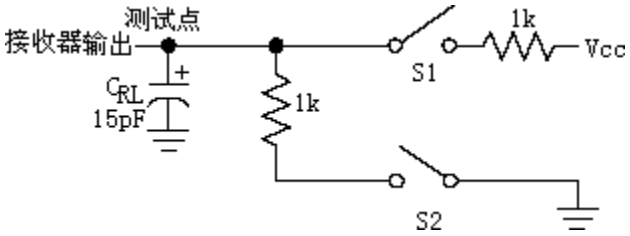


Figure 2： Receiver Enable/Disable Timing Test load

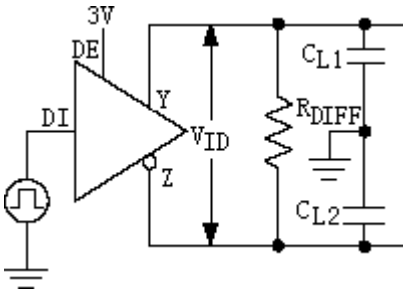


图 3：Driver Timing Test Circuit

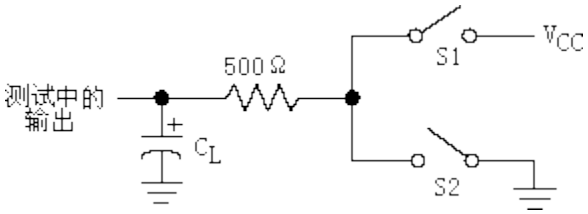


图 4：Driver Enable/Disable Timing Test Load

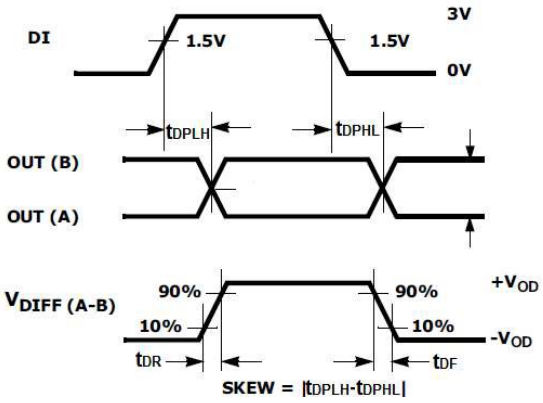


图 5：Driver Propagation Delays

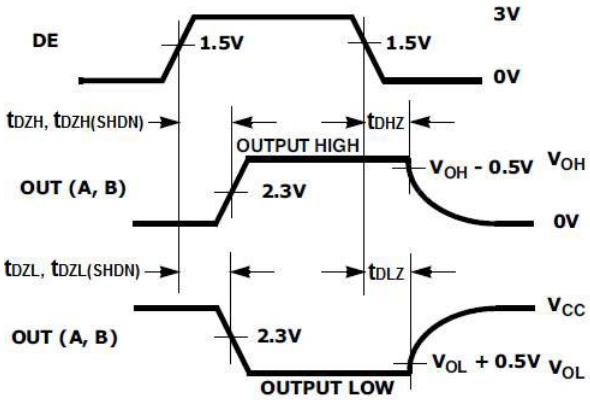


图 6：Driver Enable and Disable Times

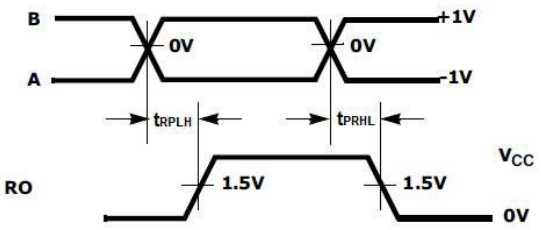


Figure 7： Receiver Propagation Delays

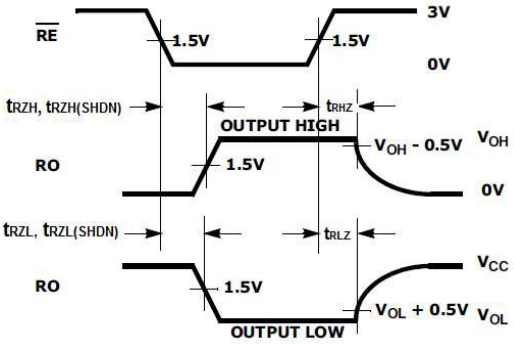


Figure 8： Receiver Enable and Disable Times

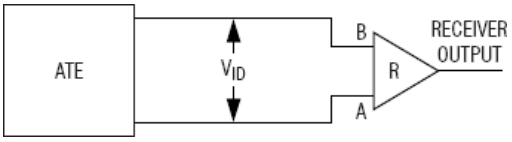


Figure 9： Receiver Propagation Delay Test Circuit

Typical Application Diagram

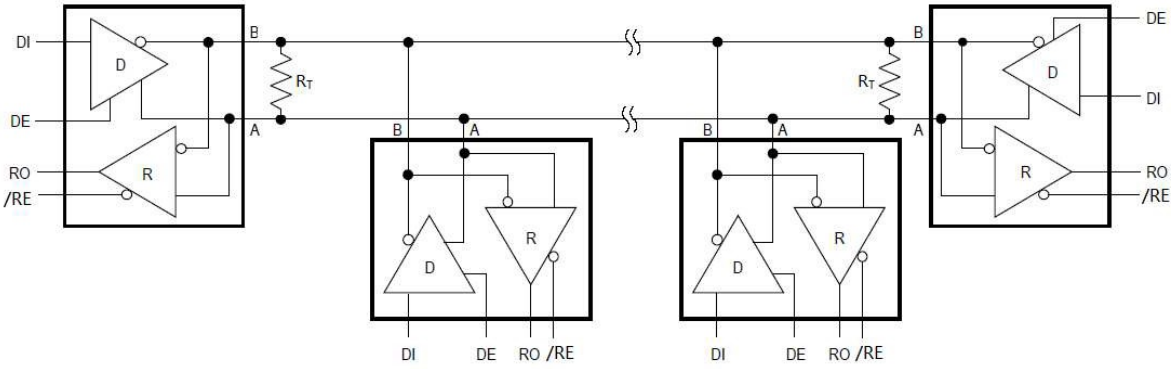
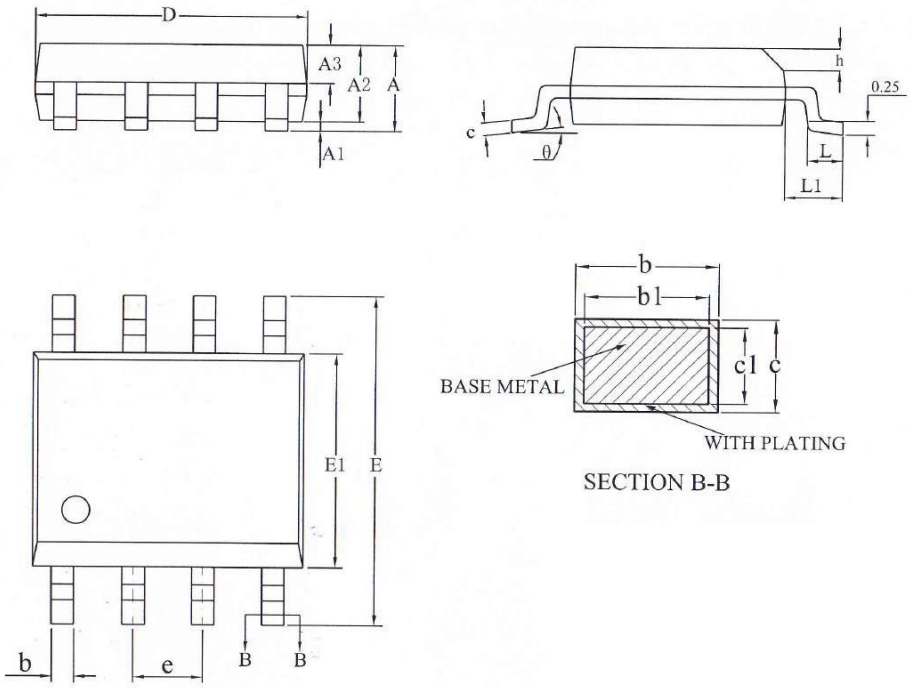


Figure 10 Typical half-duplex RS-485 network

Package size (SOP8)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	—	0.48
b1	0.38	0.41	0.44
c	0.20	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°