BL0940 datasheet

BL0940 Calibration-Free Metering Chip Data Sheet

Version update instructions

Version	date	content	Revised by
V1.0	2018/09/07	create	Liao Kang, HCJ
V1.1	2019/12/25	Errata	Liao Kang, HCJ

Table of contents

1 Product description

1.1 Function introduction

BL0940 is a calibration-free energy metering chip with a built-in clock. It is suitable for applications such as single-phase multi-function energy meters, smart sockets, smart home appliances, and electric bicycle charging piles. It has a high cost performance.

BL0940 integrates 2 - way high-precision Sigma-Delta ADC , analog circuit modules such as reference voltage, power management, and digital signal processing circuits for processing electrical parameters such as active power, current and voltage RMS.

BL0940 can measure current, voltage RMS, active power, active energy and other parameters, and can output fast current RMS (for leakage monitoring or overcurrent protection) , as well as temperature detection, waveform output and other functions, output through UART/SPI interface The data can fully meet the needs of smart sockets, smart home appliances, single-phase multi-functional electric energy meters, electric bicycle charging piles, and big data collection of electricity consumption information.

BL0940 has a patented anti-creep design, combined with a reasonable external hardware design, it can ensure that the noise power is not included in the energy pulse when there is no current.

1.2 main feature

- Two independent Sigma-Delta ADCs , one current and one voltage.
- RMS current range (10mA~35A) @1mohm
- Active energy (1w~7700w) @1mohm@220V
- Can output current, voltage RMS, fast current RMS, active power, current and voltage waveform phase angle
- batch factory gain error is less than 1% , and the external components can be exempted from calibration if they meet certain conditions
- current channel has a leakage /overcurrent monitoring function, and the monitoring threshold and response time can be set
- Voltage zero-crossing signal output
- Built-in waveform register, which can output waveform data for load type analysis
- Integrated temperature sensor to meet the needs of product over-temperature monitoring,

high-current node preset temperature alarm, ambient temperature measurement, etc.

- Integrated SPI (the fastest rate supports 900KHz) / UART (4800bps) communication method
- Power down monitoring, below 2.7V , the chip enters the reset state
- Built-in 1.218V reference voltage source
- Built-in oscillation circuit, the clock is about 4MHz
- Chip single working power supply 3.3V , low power consumption 10mW (typical value)
- TSSOP14 encapsulation

1.3 System Block Diagram

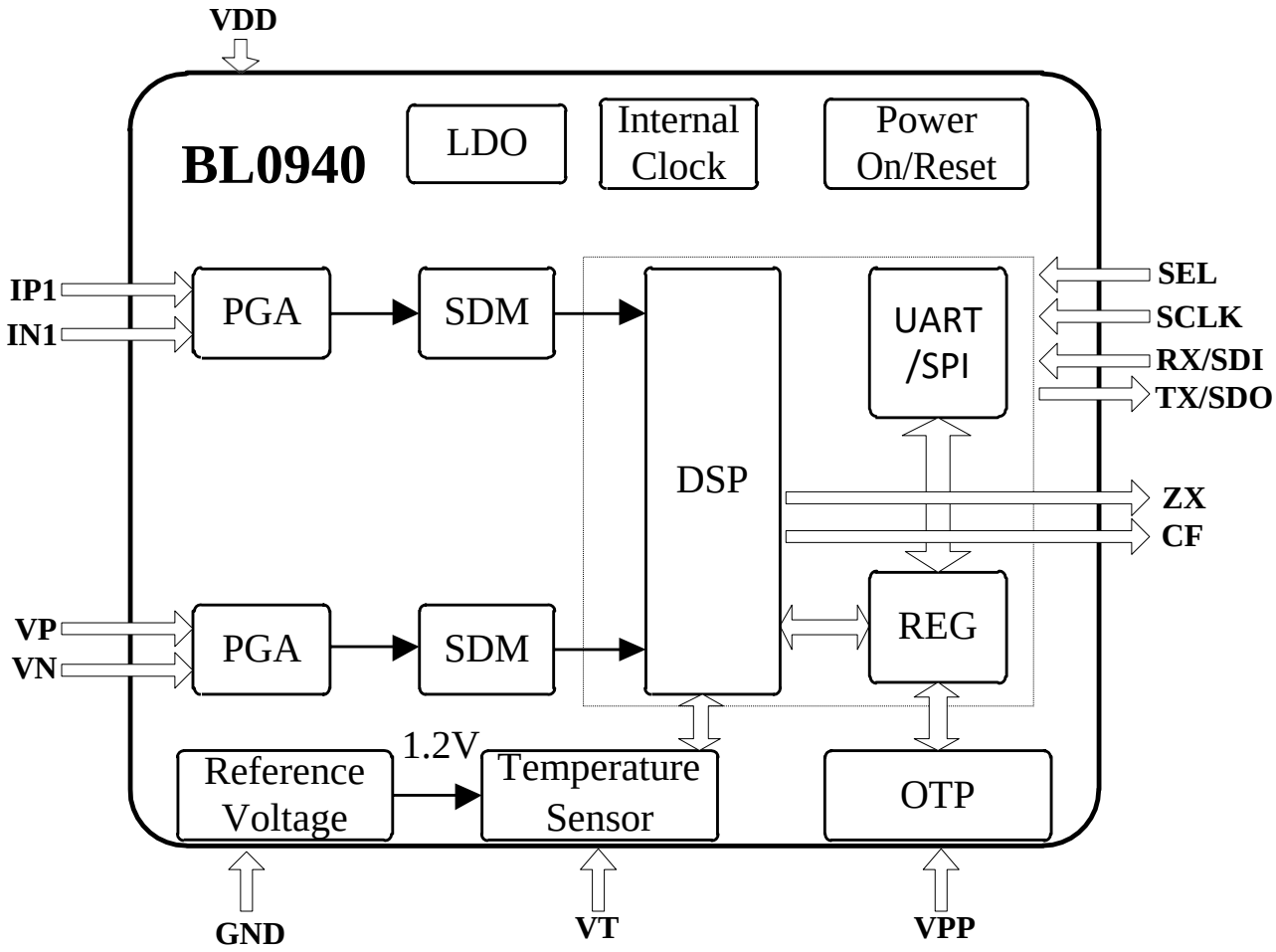


Figure 1

1.4 Package and Pin Description

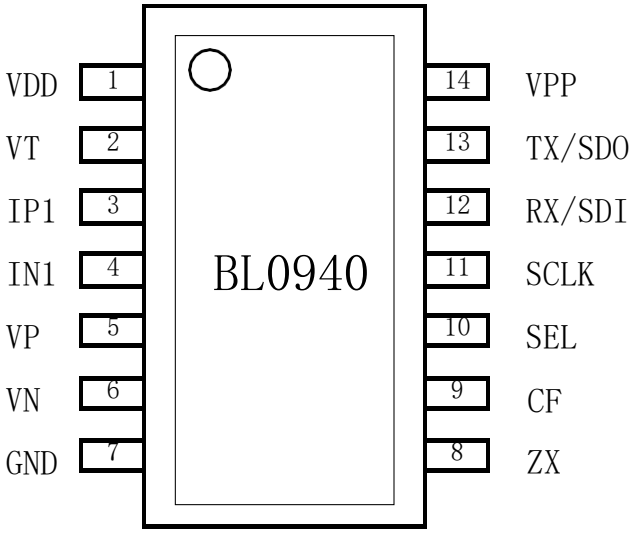


Figure 2

Pin Description (TSSOP14)

pin number	symbol	illustrate
1	VDD	Power supply (+3.3V)
2	VT	External temperature sensor signal input
3,4	IP1, IN1	Analog input of the current channel, the maximum differential voltage of the pins is ±50mV (35mV rms)
5,6	VP,VN	Voltage signal input terminal, maximum differential voltage ±100mV (70mV rms)
7	GND	chip ground
8	ZX	Voltage zero-crossing indication
9	CF	Energy pulse output, see the description of the MODE register for the multiplexing function
10	SEL	UART/SPI Communication mode selection (0: UART 1: SPI), internal pull- down resistor, Floating is 0 level (UART) , and the pin is directly connected to VDD to be high level (SPI)
11	SCLK	SPI mode clock input; in UART communication mode, it can be suspended
12	RX/SDI	UART/SPI multiplexing pin, UART RX/SPI DIN
13	TX/SDO	UART/SPI multiplexing pin, UART TX/SPI DOUT, requires an external pull-up resistor
14	VPP	Keep it in the air

1.5 register list

address	name	external read/write	internal read/write	bit width	Defaults	describe
Electric parameter register (read only)						
0x00	I_FAST_RMS	R	W	twenty four	0x000000	Current Fast RMS Register, Unsigned
0x01	I_WAVE	R	W	twenty four	0x000000	Current waveform register, signed
0x03	V_WAVE	R	W	twenty four	0x000000	Voltage waveform register, signed
0x04	I_RMS	R	W	twenty four	0x000000	Current RMS register, unsigned
0x06	V_RMS	R	W	twenty four	0x000000	Voltage rms register, unsigned
0x08	WATT	R	W	twenty four	0x000000	Active power register, signed
0x0A	CF_CNT	R	W	twenty four	0x000000	Active energy pulse count, unsigned
0x0C	CORNER	R	W	16	0x0000	Current Voltage Waveform Phase Angle Register
0x0E	TPS1	R	W	10	0x000	Internal temperature detection register, unsigned
0x0F	TPS2	R	W	10	0x000	External temperature detection register, unsigned
User operation register (read and write)						
0x10	I_FAST_RMS_CTRL	R/W	R	16	0xFFFF	Current Fast RMS Control Register
0x13	I_RMSOS	R/W	R	8	0x00	Current RMS Small Signal Correction Register
0x15	WATTOS	R/W	R	8	0x00	Power Small Signal Correction Register
0x17	WA_CREEP	R/W	R	8	0x0B	Active power anti-passage register

0x18	MODE	R/W	R	16	0x0000	User Mode Select Register
0x19	SOFT_RESET	R/W	R	twenty four	0x000000	When writing 0x5A5A5A, the user area register is reset
0x1A	USR_WRPROT	R/W	R	8	0x00	User write-protect setting register. After writing 0x55 , the user operation register can be written; to write other values, use The user operation register area cannot be written
0x1B	TPS_CTRL	R/W	R	16	0x07FF	Temperature Mode Control Register
0x1C	TPS2_A	R/W	R	8	0x0000	External Temperature Sensor Gain Coefficient Correction Register
0x1D	TPS2_B	R/W	R	8	0x0000	External Temperature Sensor Offset Coefficient Correction Register

1.6 Special Register Description

1.6.1 User Mode Select Register

0x18	MODE	Operating Mode Register		
No.	name	default value	description	
[7:0]	reserved	0b00000000	reserve	
8	RMS_UPDATE_SEL	0b0	RMS register refresh time selection choose	0: 400ms 1: 800ms
9	AC_FREQ_SEL	0b0	AC frequency selection	0: 50Hz 1: 60Hz
[11:10]	reserved	0b00	reserve	
12	CF_UNABLE	0b0	CF pin output function selection	0: reserved 1: Overcurrent alarm function TPS_CTRL[14] configuration efficient
[15:13]	reserved	0b000	reserve	

1.6.2 Temperature Mode Control Register

0x1B	TPS_CTRL	Temperature Mode Control Register		
No.	name	default value	description	
0x1B	TPS_CTRL	0x07FF	[15] Temperature measurement switch, default 0b0, open Start measuring temperature	0: open
				1: off
			[14] Alarm switch, default 0b0,	0: Temperature alarm is on
				1: Current channel overcurrent/leakage alarm turn on
			[13:12] Temperature measurement selection, default 0b00 automatic temperature measurement	00: automatic temperature measurement
				01: Same as 00
				10: Internal temperature measurement
				11: External temperature measurement
			[11:10] Temperature measurement time interval selection, default 0b01 100ms	00: 50ms
				01: 100ms
				10: 200ms
				11: 400ms
			[9:0] External temperature measurement alarm threshold setting Set, the default setting is 0x3FF, no alarm	The TPS2 register value is greater than or equal to the report Alarm value, generate an alarm

1.7 Performance

1.7.1 Electrical parameter performance

（ VDD =3.3V， GND = 0V， on-chip reference voltage source, built-in crystal oscillator, 25 ℃, electric energy is measured through CF output）

Measurement items	symbol	Measurement conditions	the smallest	typical	maximum	unit
Power supply VDD	VDD		3.0		3.6	V
power consumption	Iop	VDD=3.3V		3		mA
Measuring range		4000:1 input drive state range				
Active energy measurement accuracy (big signal)		35A~100mA output Into @ 1mohm sampling resistor		0.2		%
Active energy measurement accuracy (small signal)		100mA~50mA input @ 1mohm sampling resistance		0.4		%
Active energy measurement accuracy (tiny signal)		50mA~10mA input Into @ 1mohm sampling resistor		0.6		%
RMS measurement accuracy (big signal)		35A~100mA input @ 1mohm sampling resistance		0.2		%
RMS measurement accuracy (small signal)		100mA~50mA input @ 1mohm sampling resistance		2		%
RMS measurement accuracy (tiny signal)		50mA~10mA input @ 1mohm sampling resistance		6		%
Fast RMS response	50Hz	Can be set to	10		40	M

time	60Hz	cycle/ half cycle	8.3		33	M
Zero-crossing signal output delay				571		u
The phase angle between channels causes measurement errors Poor (capacitive)	PF08err	Phase lead 37 (PF=0.8)			0.5	%
The phase angle between channels causes measurement errors Poor (sensibility)	PF05err	Phase lag 60 (PF=0.5)			0.5	%
AC Power Supply Rejection (Output Frequency rate amplitude change)	ACPSRR	IP/N=100mV			0.1	%
DC supply rejection (output frequency rate amplitude change)	DCPSRR	VP/N=100mV			0.1	%

Measurement items	symbol	Measurement conditions	the smallest	typical	maximum	unit
Analog input level (current)		Current differential input (peak)			50	mV
Analog input level (voltage)		Voltage differential input (peak)			200	mV
Analog input impedance				370		kΩ
SEL pull-down resistor		SEL (pull down)		56.9		kΩ
Analog input bandwidth		(-3dB)		3.5		kHz
Internal Voltage Reference	Vref			1.218		V
logic input high		VDD=3.3V±5%	2.6			V
Logic input low		VDD=3.3V±5%			0.8	V
logic output high		VDD=3.3V±5% IOH=5mA	VDD-0.5			V
Logic output low level		VDD=3.3V±5% IOL=5mA			0.5	V

1.7.2 limit range

（T = 25° C）

project	symbol	extremum	unit
Power supply voltage VDD	VDD	-0.3 ~ +4	V
Analog input voltage (relative to GND)	IP1, VP	-4 ~ +4	V
Digital input voltage (relative to GND)	UART_SEL, RX/SDI	-0.3 ~ VDD+0.3	V
Digital output voltage (relative to GND)	CF, TX/SDO	-0.3 ~ VDD+0.3	V
Operating temperature	Topr	-40 ~ +85	℃
storage temperature	Tstr	-55 ~ +150	℃

2 Functional description

BL0940 is mainly divided into two parts: analog signal processing and digital signal processing. The analog part mainly includes two-channel PGA, two-channel Sigma-Delta ADC, built-in clock (internal clock), power on/reset monitoring (Power on/reset), temperature detection (temperature sensor), LDO and other related analog modules, and the digital part is a digital signal processing module (DSP).

2.1 Current and voltage transient waveform measurement

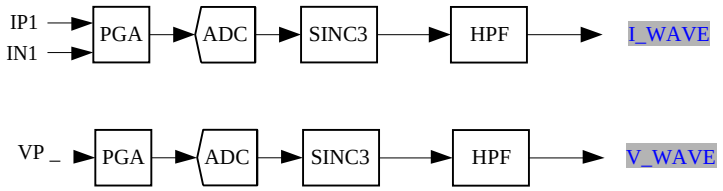


Figure 4

As shown in the figure above, the current and voltage pass through the analog module amplifier (PGA) and high-precision analog-to-digital conversion (ADC) respectively to obtain two 1- bit PDMs for the digital module, and the digital module passes through the down-sampling filter (SINC3), high-pass filter (HPF), channel offset correction and other modules to obtain the required current waveform data and voltage waveform data (I_WAVE, V_WAVE).

The collected load current and voltage waveform data are updated at a rate of 7.8k, each sampled data is a 24bit signed number, and stored in the waveform register (I_WAVE, V_WAVE) respectively, the SPI rate configuration is greater than 375Kbps, and one channel can be read continuously waveform value.

Note: The register is 24bit, if the number of digits is insufficient, high bits are filled with zeros.

addre	name	exter nal	intern al	bit	Defaults	describe

ss		read/write	read/write	width		
0x01	I_WAVE	R	W	twenty four	0x000000	Current Waveform Register
0x03	V_WAVE	R	W	twenty four	0x000000	Voltage Waveform Register

2.2 active power

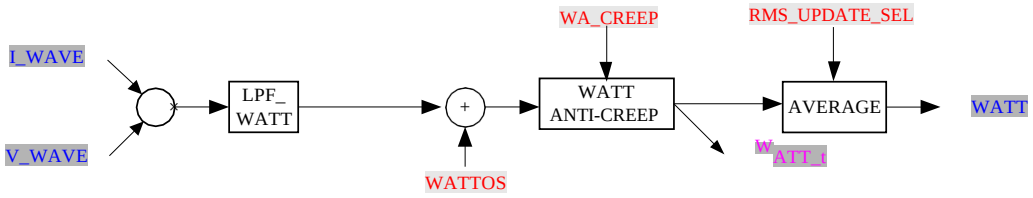


Figure 5

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x08	WATT	R	W	twenty four	0x000000	Active Power Register

Active power calculation formula： $WATT = \frac{4046*I(A)*V(V)*\cos(\varphi)}{Vref^2}$

Among them, $I(A)$, $V(V)$ is the effective value (mV) of the channel pin input signal, φ is the phase angle of the I(A) and V(V) AC signals, Vref is the built-in reference voltage, typical value 1.218V;

This register indicates whether the current active power is positive or negative, Bit[23] is the sign bit, Bit[23]=0, the current power is positive power, Bit[23]=1, the current power is negative power, complement code form.

2.3 Active Power Offset Calibration

BL0940 contains an 8 -bit active power correction register (WATTOS) , the default value

is 00H . The data in the form of 2 's complement code is used to eliminate the deviation of active power when measuring electric energy. Bit[7] is the sign bit, and the deviation here may be caused by board-level noise or crosstalk. Offset correction can make the value in the active power register close to 0 at no load .

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x15	WATTOS	R/W	R	8	0x00	Power Small Signal Correction Register

$$WATTOS = \frac{WATT - WATT0}{8 \times 3.05172}$$

WATT is the active power after correction, and WATT0 is the active power before correction.

2.4 Active power anti-creep

BL0940 has a patented power anti-submersion function, which ensures that the board-level noise power will not accumulate power when there is no current input.

active anti-creep threshold register (WA_CREEP), is an 8bit unsigned number, and the default is 0BH . The corresponding relationship between this value and the active power register value is shown in the following formula. When the absolute value of the input active power signal is less than this value, the output active power is set to 0 . This can make the value output to the active power register be 0 in the case of no load, even if there is a small noise signal, and the electric energy will not accumulate.

address	name	external	internal	bit width	Defaults	describe
		read/write	read/write			
0x17	WA_CREEP	R/W	R	8	0x0B	Active power anti-passage register

set according to the value of the power register A_WATT , and their corresponding relationship

$$WA\_CREEP = \frac{WATT}{3.0517578125*8}$$

Note: When the current channel is in the anti-skid state, the current RMS value of this channel is not measured, and it is also cut to 0 .

2.5 Energy Metering

BL0940 provides energy pulse metering. The active instantaneous power can be integrated for a period of time to obtain active energy, and can further output the calibration pulse CF. The CF_CNT register stores the number of output energy pulses CF, as shown in the figure below.

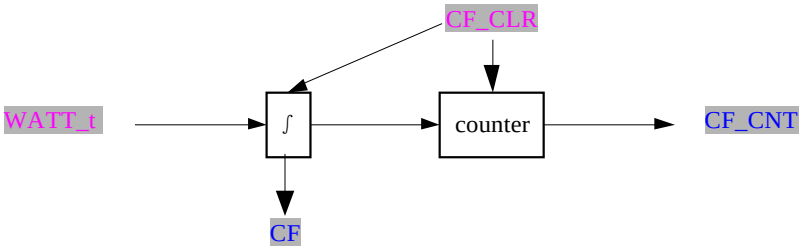


Figure 6

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x0A	CF_CNT	R	W	twenty four	0x000000	Active energy pulse count, unsigned

Active energy pulse counting can also directly count the number of pulses from the CF pin through the I/O interrupt . When the cycle of CF is less than 180ms, it is a pulse with a 50% duty cycle. When it is greater than or equal to 180ms, the high power Flat fixed pulse width 90ms.

Note: The CFA_CNT register is the algebraic and accumulation method of electric energy pulses, that is, positive power is added and negative power is subtracted.

The accumulation time for each CF pulse $t_{CF} = \frac{1638.4*256}{WATT}$

Where WATT is the corresponding active power register value (WATT).

2.6 RMS value of current and voltage

The effective value of the two channels, as shown in the figure below, passes through the square circuit (X^2) , low-pass filter (LPF_RMS) , and root circuit (ROOT) to obtain the instantaneous value RMS_t of the effective value , and then obtains the average of the two channels by averaging value (I_RMS and V_RMS) .

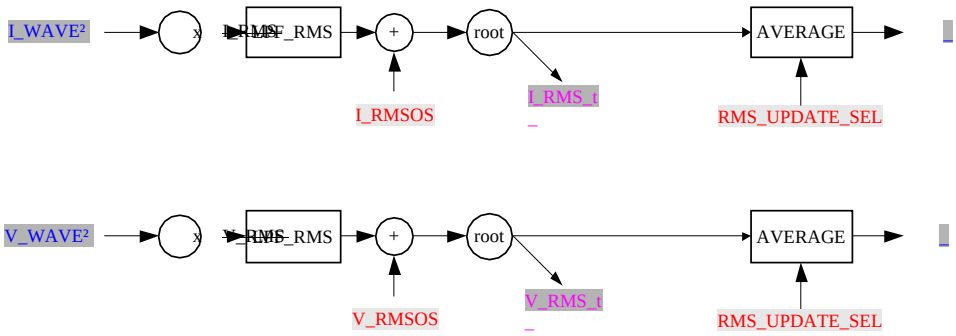


Figure 7

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x04	I_RMS	R	W	twenty four	0x000000	Current RMS register, unsigned
0x06	V_RMS	R	W	twenty four	0x000000	Voltage rms register, unsigned

0x18	MODE	Operating Mode Register		
No.	name	default value	description	
8	RMS_UPDATE_SEL	0b0	When the rms register is refreshed time setting	0: 400ms 1: 800ms

Set MODE[8].RMS_UPDAT_SEL, you can choose the average refresh time of the effective value to be 400ms or 800ms , and the default is 400ms . When the channel is in the

anti-submarine state, the effective value of the current channel is zero.

Current RMS conversion formula: I_RMS = $\frac{324004*I(A)}{Vref}$

Voltage RMS conversion formula: V_RMS = $\frac{79931*V(V)}{Vref}$

$Vref$ is the reference voltage, the typical value is 1.218V.

Note: I(A) is the input signal (mV) between IP1 and IN1 pins , V(V) is the input signal (mV) of VP pin .

2.7 Current Voltage RMS Offset Calibration

BL0940 contains an 8 -bit effective value offset register (I_RMSOS), the default value is 00H , and the deviation in the effective value calculation is adjusted with the data in the form of 2 's complement . Bit[7] is a sign bit, this deviation may come from input noise, and deviation correction can make the value in the effective value register close to 0 under no-load conditions .

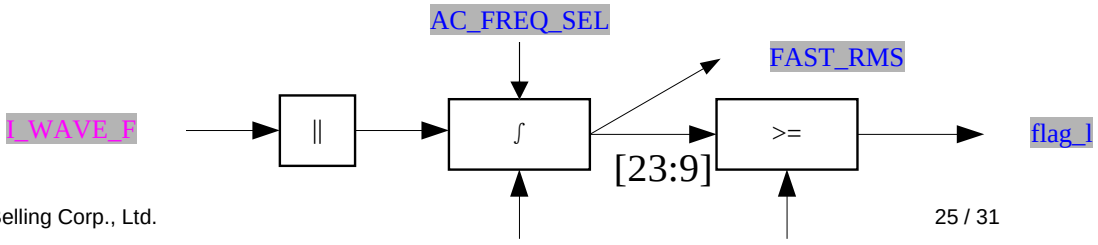
address	name	external read/write	internal read/write	bit width	Defaults	describe
0x13	I_RMSOS	R/W	R	8	0x00	Current RMS Small Signal Correction Register

Calibration formula : $RMSOS = \frac{RMS^2 - RMS0^2}{9.3132 \times 2^{15}}$

Here RMS0 is the effective value before correction, and RMS is the effective value after correction.

2.8 Leakage / overcurrent detection

BL0940 has a fast RMS register, which can detect half cycle or cycle RMS. This function can be used for leakage or overcurrent detection. For the source of the leakage waveform L_WAVE , refer to the channel waveform block diagram. After taking the absolute value of I_WAVE_F , the half cycle or cycle time is accumulated, which is determined by FAST_RMS_CTRL[15] selection, default value 1 selects cycle accumulation, the longest response time is 40ms (50Hz) or 33mS (60Hz) , pay attention to x_FAST_RMS during half cycle accumulation The jump of the register is relatively large. To distinguish 50 Hz and 60Hz __ half cycle time (AC_FREQ_SEL).



FAST_RMS_CTRL [15]	FAST_RMS_CTRL [14:0]

Figure 8

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x10	I_FAST_RMS_CTRL	R/W	R	16	0xFFFF	Current Fast RMS Control Register

Through the I_FAST_RMS_CTRL fast RMS control register, the refresh time can be selected as half cycle or cycle, and the fast RMS threshold (that is, the leakage or overcurrent threshold) can be set.

0x10	MODE	Fast RMS Register		
No.	name	default value	description	
0x10	I_FAST_RMS_CTRL	0xFFFF	[15] Current Fast RMS Register Refresh Time	0: half cycle 1: Cycle
			[14:0] Current Fast RMS Threshold	

0x18	MODE	Operating Mode Register		
No.	name	default value	description	
9	AC_FREQ_SEL	0b0	AC frequency selection	0: 50Hz 1: 60Hz

Set AC frequency by MODE[9].

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x00	I_FAST_RMS	R	W	twenty four	0x000000	Current fast rms, unsigned

24 -bit unsigned fast effective value register according to the cycle or half cycle , compare Bit[23:9] of the FAST_RMS register with the leakage / overcurrent threshold FAST_RMS_CTRL [14:0] , if it is greater than or equal to the set threshold, the leakage / Overcurrent alarm output indicates that the pin outputs a high level .

leakage /overcurrent alarm output indication pin is CF, you need to set MODE[12]=1 first, and then set TPS_CTRL[14]=1.

0x18	MODE	Operating Mode Register		
No.	name	default value	description	
12	CF_UNABLE	0b0	CF pin output selection	0: Energy pulse MODE[11] configuration is valid
				1: Temperature measurement/leakage alarm TPS[14] configuration is valid

0x1B	TPS_CTRL	Temperature Mode Control Register		
No.	name	default value	description	
14	ALERT_CTRL	0b0	alarm switch	0: Temperature alarm is on
				1: Overcurrent/leakage alarm is on

Since the fast effective value is updated by cycle or half cycle, the longest interrupt response time is 2 cycles or 2 half cycles.

2.9 Phase angle calculation

BL0940 can be used for phase angle measurement, and the phase angle CORNER between the current and the voltage indicates the reactive quadrant. The calculation is obtained by the positive zero-crossing time difference between the current and the voltage. When the current is positive zero-crossing, it is updated to the register CORNER, and the register is a 16-bit unsigned number.

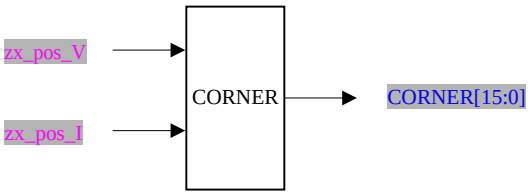


Figure 9

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x0C	CORNER	R	W	16	0x0000	Current Voltage Waveform Phase Angle Register

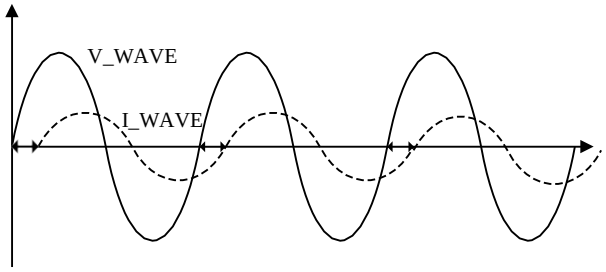


Figure 10

Phase angle conversion formula: unit is radian

$$2*pi*CORNER*\frac{f_c}{f_0}$$

Among them, f_c is the measurement frequency of the AC signal source, the default is 50Hz, f_0 is the sampling frequency, the typical value is 1MHz

2.10 Zero-crossing detection

BL0940 provides voltage zero-crossing detection, and the zero-crossing signal is directly output from the pin ZX. ZX is 0, which means the positive half cycle of the waveform, and ZX is 1, which means the negative half cycle of the waveform. The time delay with the actual input signal is 570us.

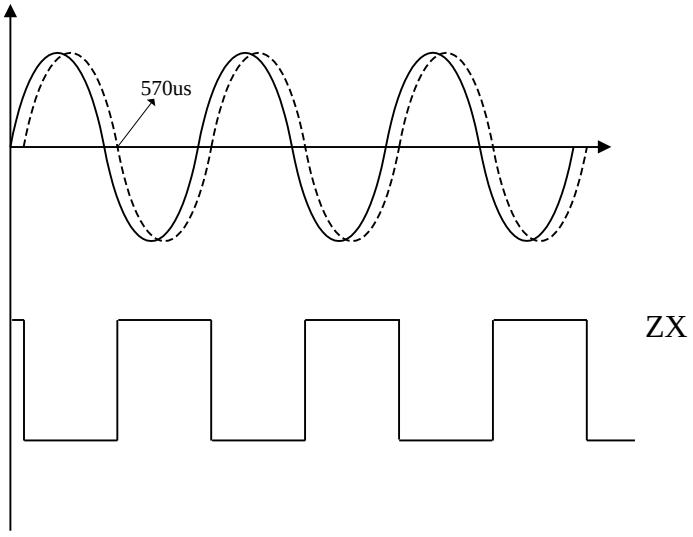


Figure 11

2.11 Thermometer

BL0940 provides internal temperature measurement and off-chip temperature measurement.

When the external temperature is measured, the optional output alarm indication, when the alarm function is turned on, the CF pin selects the output alarm signal, when TPS2 is greater than or equal to the alarm threshold, the CF pin outputs a high level, and the temperature indication alarms. When the temperature value is lower than the alarm value or the alarm function is turned off, the alarm indication will be exited.

0x1B	TPS_CTRL	Temperature Mode Control Register		
No.	name	default value	description	
0x1B	TPS_CTRL	0x07FF	[15] Temperature measurement switch, default 0b0, open Start measuring temperature	0: open
				1: off
			[14] Alarm switch, default 0b0,	0: Temperature alarm is on
				1: Current channel overcurrent/ Leakage alarm on
			[13:12] Temperature measurement selection, default 0b00 automatic temperature measurement	00: automatic temperature measurement
				01: Same as 00
				10: Internal temperature measurement
				11: External temperature measurement
			[11:10] Temperature measurement time interval selection, default 0b01 100ms	00: 50ms
				01: 100ms
				10: 200ms
				11: 400ms
			[9:0] External temperature measurement alarm threshold setting set, the default setting is 0x3FF	

First set MODE[12]=1, and then set TPS_CTRL[14]=0, the CF pin can be turned on to output an

external temperature alarm indicator.

0x18	MODE	Operating Mode Register		
No.	name	default value	description	
12	CF_UNABLE	0b0	CF pin output selection	0: Energy pulse MODE[11] configuration is valid
				1: Temperature measurement alarm TPS[14] configuration is valid

External and internal temperature readings are stored in two registers, TPS1 and TPS2, respectively.

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x0E	TPS1	R	W	10	0x0000	Internal temperature value register, unsigned
0x0F	TPS2	R	W	10	0x0000	External temperature value register, unsigned

Internal temperature measurement formula: Tx=(170/448)(TB/2-32)-45

TB is the TPS1 register value.

The external test temperature adopts SAR ADC, that is, the maximum input signal of the VT pin is VDD/2 (V), and the TPS2 register is the corresponding D sampled value, full scale 1024,

address	name	external read/write	internal read/write	bit width	Defaults	describe
0x1C	TPS2_A	R/W	R	8	0x00	External Temperature Sensor Gain Coefficient A Correction Register
0x1D	TPS2_B	R/W	R	8	0x00	External Temperature Sensor Bias Coefficient B Correction Register

3 Communication Interface

register data is sent in 3 bytes (24bit). For the register data less than 3 bytes, the unused bits are filled with 0, and 3 bytes are sent.

3.1 SPI

- Through the pin UART_SEL choose , with UART reuse
- ●♦●♋❖♏ mode
- Half-duplex communication , the communication rate can be configured , the maximum communication rate 900khz
- 8-bit data transfer, MSB First , LSB is behind
- ●☞♓☒ a clock polarity / phase (CPOL=0, CPHA=1)

3.1.1 Operating mode

The master device works in Mode1: CPOL=0, CPHA=1, that is, in the idle state, SCLK is at low level, and data transmission is at the first edge, that is, the transition of SCLK from low level to high level, So data sampling is on the falling edge, and data transmission is on the rising edge.

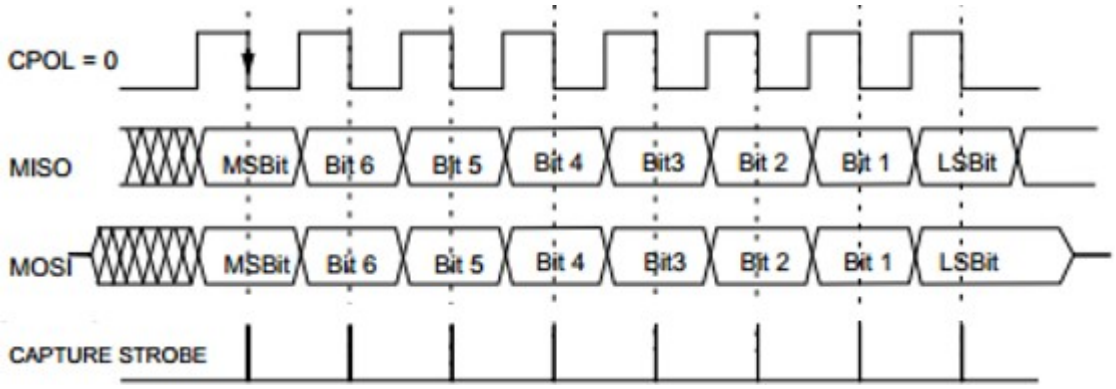


Figure 12

3.1.2 frame structure

In the communication mode, first send 8bit identification byte (0x58) or (0xA8), (0x58) is the identification byte of read operation, (0xA8) is the identification byte of write operation , and then send the register address byte to decide to access the register address (see BL0940 Register List) . The figure below shows the data transfer sequence for read and write operations, respectively. After a frame of data transmission is completed, BL0940 re-enters the communication mode. The number of SCLK pulses required for each read / write operation is 48 bits.

There are two frame structures, which are described as follows:

1) Write operation frame

write frame	0xA8	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

Among them, the checksum byte CHECKSUM is((0xA8 + ADDR + DATA_H + DATA_M+ DATA_L) &0xFF) and then reversed bit by bit. 2) Read operation frame

read command frame	0x58	ADDR[7:0]

return data	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

Among them, the checksum byte CHECKSUM= ((0x58 + ADDR + DATA_H + DATA_M+ DATA_L) & 0xFF) is reversed bit by bit. Note: The data is a fixed 3 bytes (the high byte is in front, the low byte is in the back, if the valid byte of the data is less than 3 bytes, the invalid bit is filled with 0)

3.1.3 Write Operation Timing

The serial write sequence is performed as follows. The frame identification byte {0xA8} indicates that the data communication operation is writing data. ADDR is the address of the register that needs to write data. The MCU will prepare the data bits that need to be written into the BL0940 before the falling edge of SCLK , and start shifting in the register data at the falling edge of

the clock of SCLK. All remaining bits of the register data are also shifted left on this falling edge of SCLK (Figure 13).

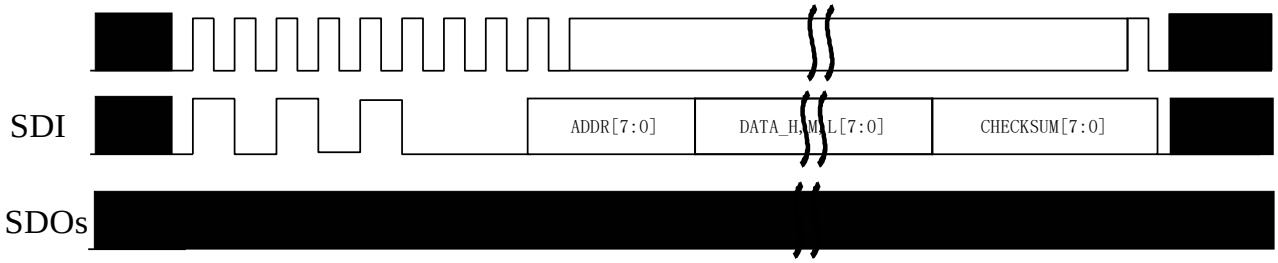


Figure 13

3.1.4 Read Operation Timing

During the data read operation of BL0940 , at the rising edge of SCLK , BL0940 outputs the corresponding data bit to the SDO logic output pin, and the SDO value remains unchanged during the next SCLK is 1 , that is, in the next On the falling edge, an external device can sample the SDO value. When performing data read operation, MCU must first send a read command frame.

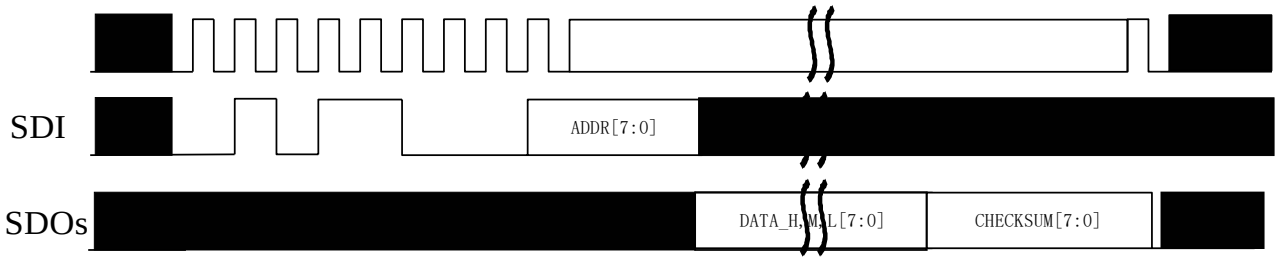


Figure 14

When BL0940 is in the communication mode, the frame identification byte {0x58} indicates that the data communication operation is read data. Then the following byte ADDR is the address of the target register to be read. After the BL0940 receives the register address, it starts to shift out the data in the register on the rising edge of SCLK (Figure 14) . All remaining bits of the register data are shifted out on subsequent SCLK rising edges. Therefore, on the falling edge, the external device can sample the output data of the SPI . Once the read operation is complete, the serial interface re-enters communication mode. At this time, the SDO output enters a high-impedance state on the falling edge of the last SCLK signal.

3.1.5 SPI Interface fault tolerance mechanism

The soft reset function of the SPI interface can reset the SPI interface independently by sending 6 bytes of 0xFF through the SPI interface .

3.2 UART

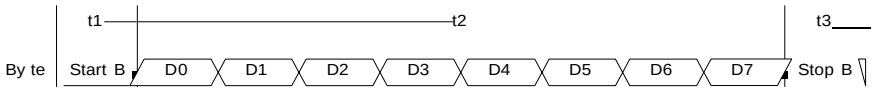
3.2.1 overview

BL0940 can use UART communication. The UART interface only needs two low-speed optocouplers to realize isolated communication. Fixed baud rate 4800bps, N, 8, 1.5, working in slave mode, half-duplex communication.

3.2.2 describe

UART port settings: communication baud rate 4800bps, no parity, stop bit 1.5;

3.2.3 format per byte



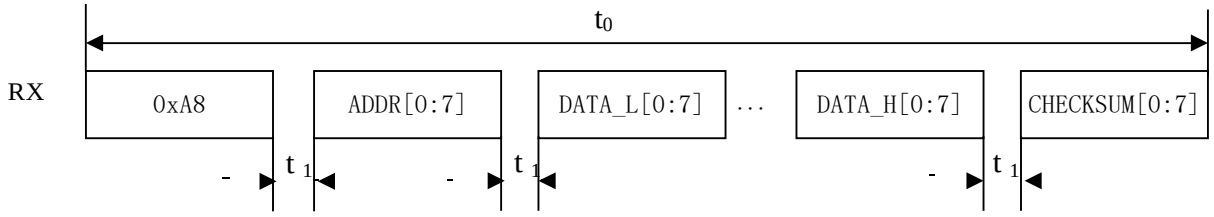
Start bit low level duration t1=208us;

Valid data bit time lasts t2=208*8=1664us

Stop bit high level duration t3=208us+104us

3.2.4 write timing

host UART write data sequence is shown in the figure below. The host first sends the command byte (0xA8), then sends the register byte (ADDR) to be written into the data, and then sends the data byte in sequence (low byte first, high byte first) After the byte, the valid byte of the data is less than 3 bytes, and the invalid bit is filled with 0), and the last checksum byte.

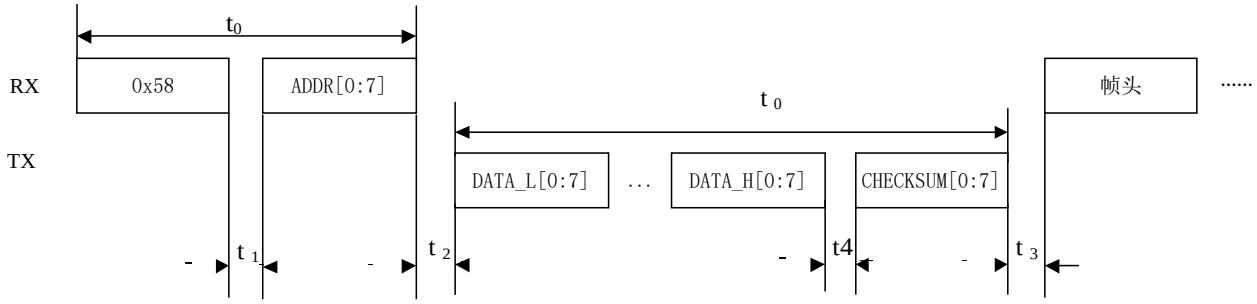


(0xA8) is the frame identification byte of the write operation, and ADDR is the internal register address of the BL0940 corresponding to the write operation .

CHECKSUM byte is ((0xA8+ADDR+Data_L+Data_M+Data_H) & 0xFF) and then reversed bit by bit.

3.2.5 read timing

host UART reading data is shown in the figure below. The host first sends the command byte (0x58), then sends the register address byte (ADDR) to be read, and then BL0940 sends data bytes in sequence (low byte first, high byte first) After the byte, the valid byte of the data is less than 3 bytes, and the invalid bit is filled with 0), and the last checksum byte.



(0x58) is the frame identification byte of the read operation, and ADDR is the internal register address of the BL0940 corresponding to the read operation .

CHECKSUM byte is ((0x58+ADDR+Data_L+Data_M+Data_H) & 0xFF) and then reversed bit by bit. Timing description:

	说明	Min	Type	Max	Unit
t1	MCU 发送字节间的间隔时间	0		20	mS
t2	读操作时 MCU 发送寄存器地址结束到 BL0940 发送字节的间隔时间		72		uS
t3	帧间隔时间	0.5			uS
t4	BL0940 发送字节之间的间隔时间		116		uS

3.2.6packet sending mode

By command "(0x58)+0xAA",BL0940 A data packet of all electric parameters will be returned. The returned packets totaled 35 bytes, 4800 bps takes 77ms. The specific format is: Baotou (1byte head) → Current fast effective value (3byte I_FAST_RMS) → Current effective value (3byte I_RMS) →☼ℳ♦ℳ❒❖ℳ♎ (3byte) →✞□●♦♋♑ℳ effective value (3byte V_RMS) →☼ℳ♦ℳ❒❖ℳ♎ (3byte) →🏳□♦ℳ❒ value (3byte WATT) →☼ℳ♦ℳ❒❖ℳ♎ (3byte) →🏳◆●♦ℳ count value (3byte CF_CNT) →☼ℳ♦ℳ❒❖ℳ♎ (3byte) →✋■♦ℳ❒■♋● temperature measurement value (2byte TPS1 + 1byte 0) → External temperature sensor measurement value (2byte TPS2 + 1byte 0)

→ Checksum value (1byte CHECKSUM). Full electric parameter

package format:

名称	字节序号	内容	名称	字节序号	内容
包头	0	Head（0x55）	保留	19	保留
I_FAST_RMS	1	I_FAST_RMS_l		20	保留
	2	I_FAST_RMS_m		21	保留
	3	I_FAST_RMS_h	CFA_CNT	22	CF_CNT_l
I_RMS	4	I_RMS_l		23	CF_CNT_m
	5	I_RMS_m		24	CF_CNT_h
	6	I_RMS_h	保留	25	保留
保留	7	保留		26	保留
	8	保留		27	保留
	9	保留	TPS1	28	TPS1_l
V_RMS	10	V_RMS_l		29	TPS1_m
	11	V_RMS_m		30	0x00
	12	V_RMS_h	TPS2	31	TPS2_l
保留	13	保留		32	TPS2_m
	14	保留		33	0x00
	15	保留	checksum	34	checksum
WATT	16	WATT_l			
	17	WATT_m			
	18	WATT_h			

checksum=((0x58+0x55+data1_l+data1_m+data1_h+.....)&0xff) then invert

3.2.7 UART Interface Protection Mechanism

The UART communication of BL0940 provides a timeout protection mechanism. If the interval between bytes exceeds 18.5mS, the UART

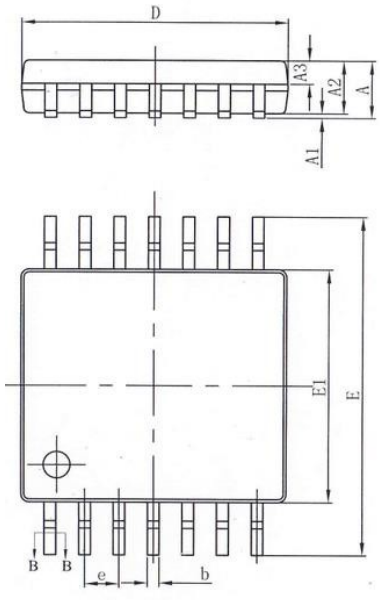
The interface resets automatically.

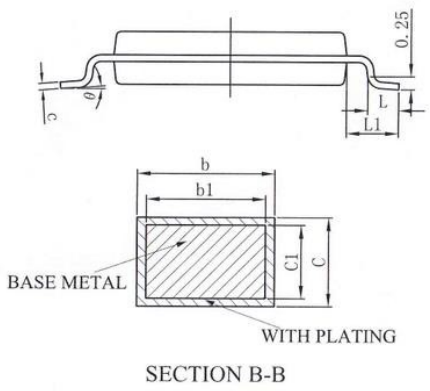
If the frame identification byte is wrong or the CHECKSUM byte is wrong, the frame data is discarded.

UART module reset: RX pin is pulled high after the low level exceeds 6.65mS, and the UART module is reset.

4 encapsulation

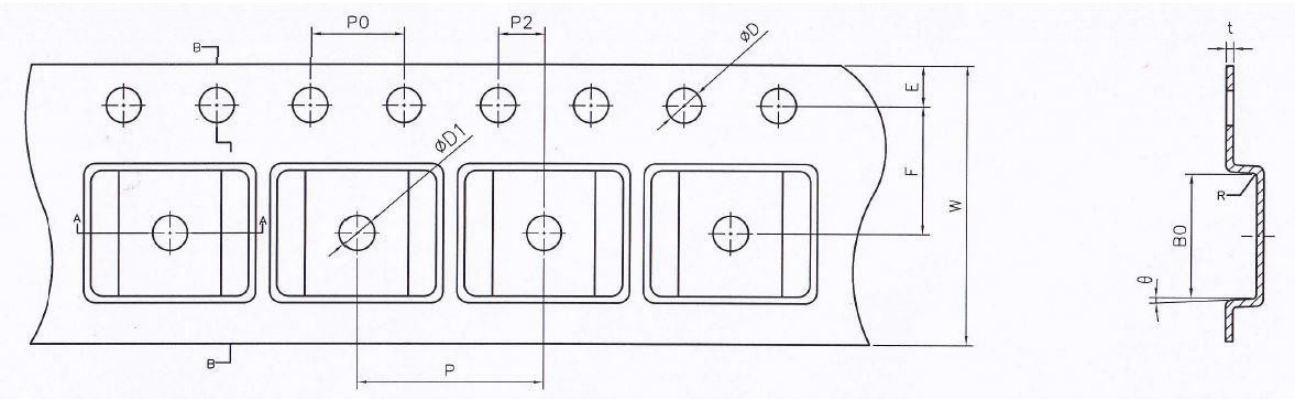
Moisture
Sensitivity
Level MSL 3
Warranty Period
Two
Years
Packing method TSSOP14
taping packing Minimum
packing 3000

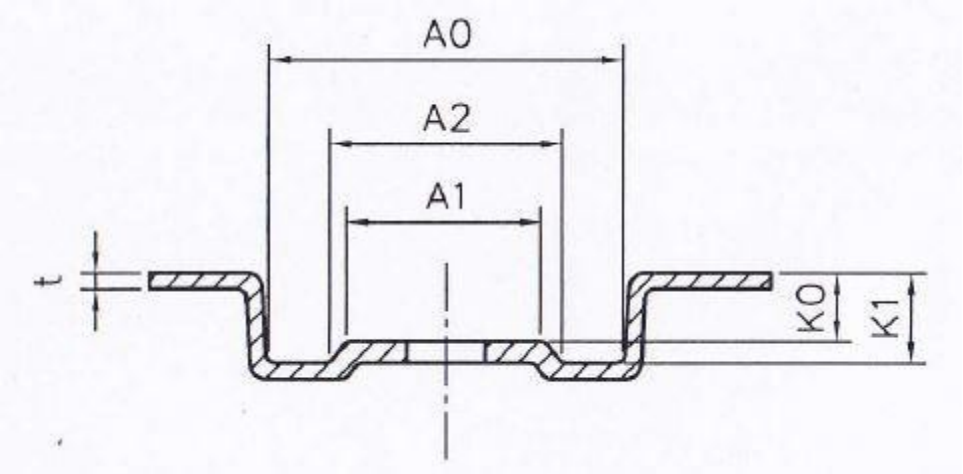




SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°





共同尺寸

外观	尺寸(mm)
E	1.75±0.1
F	5.5±0.1
P2	2.0±0.05
D	$1.5^{+0.1}_{0}$
D1	$1.5^{+0.1}_{0}$
P0	4.0±0.1
R	0.5TYP
10P0	40.0±0.20

口袋尺寸

W	12.0±0.1
P	8.0±0.1
A0	6.8±0.1
B0	5.4±0.1
K0	1.3±0.1
t	0.3±0.05
K1	1.7±0.1
A1	3.8±0.2
A2	4.4±0.2
θ	3° TYP