

BL0939

内置时钟免校准计量芯片

BL0939 datasheet

BL0939 Calibration-

Free Metering

Chip Data

Sheet





Version update

BL0939

instructions

| Vers | date | content | Revised |
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| ion | | | by |
| V1.0 | 2018/06/07 | create | Liao |
| | | | Kang, HCJ |
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| | | | Kang, HCJ |
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| | | | Kang, HCJ |



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1 Product description

1.1 Function introduction

BL0939 is a calibration-free energy metering chip with a built-in clock. It is suitable for applications such as single-phase multi-function energy meters, smart sockets, smart home appliances, and electric bicycle charging piles. It has a high cost performance.

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 $BL0939 \mbox{ integrates } 3 \mbox{ high- precision } Sigma-Delta \mbox{ ADCs} \mbox{, which can measure } 2 \mbox{ currents and } 1 \mbox{ voltage at the same time.}$

BL0939 can measure current, voltage RMS, active power, active energy and other parameters, and can output fast current RMS (for leakage monitoring or overcurrent protection), as well as temperature detection, waveform output and other functions, output through UART/SPI interface The data can fully meet the needs of smart sockets, smart home appliances, single-phase multi-functional electric energy meters, electric bicycle charging piles, and big data collection of electricity consumption information.

BL0939 has a patented anti-creep design, combined with a reasonable external hardware design, it can ensure that the noise power is not included in the energy pulse when there is no current.

1.2 main feature

- Three independent Sigma-Delta ADCs for measuring two currents and one voltage.
- RMS current range (10mA~35A) @1mohm
- Active energy (**1w~7700w**) @1mohm@220V
- Can output current, voltage RMS, fast current RMS, active power, current and voltage waveform phase angle
- batch factory gain error is less than 1%, and the external components can be exempted from calibration if they meet certain conditions
- Both current channels have leakage / overcurrent monitoring function, monitoring threshold and response time can be set
- Voltage zero-crossing signal output
- Built-in waveform register, which can output waveform data for load type analysis
- Integrated temperature sensor to meet the needs of product over-temperature monitoring, high-current node preset temperature alarm, ambient temperature measurement, etc.



integr Fastest Rate Support 900KHz / U A RT 4800 bp s communication method, U A RT Support ated SP multi-chip communication with address (SSOP20L (

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- packag
- e)
- \bullet Internal power down monitoring, below $2.7V\,,$ the chip enters the reset state.
- Built-in **1.218V** reference voltage source
- Built-in oscillation circuit, the clock is about 4MHz
- Chip single working power supply 3.3V, low power consumption 10mW (typical value)
- SSOP20L/SOP16L encapsulation



1.3 System Block Diagram

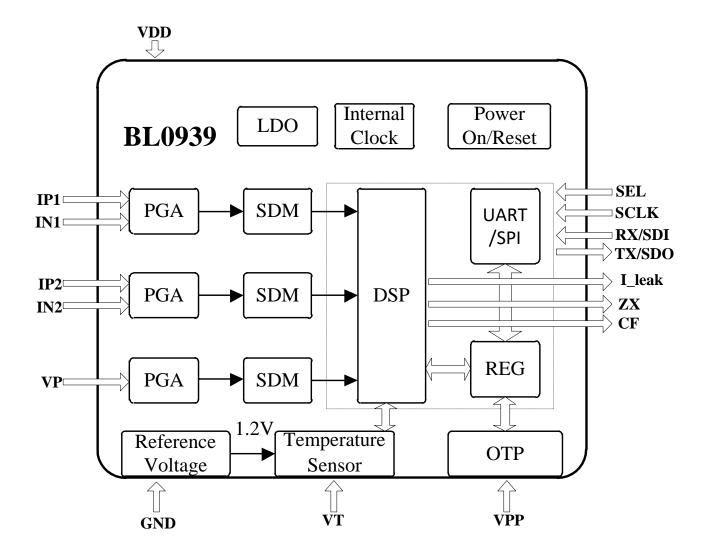
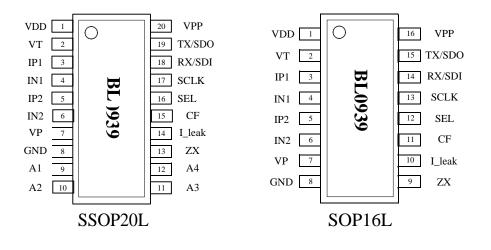


Figure 1



1.4 Package and Pin Description

The BL0939 is available in two packages.



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picture 2

pictures 3

Pin Description (SSOP20L)

| pin | symbo | illus |
|-------|----------|--|
| numbe | I | trat |
| r | | е |
| 1 | VDD | Power supply (+3.3V) |
| 2 | VT | External temperature sensor signal input |
| 3,4 | IP1, IN1 | Analog input of the current A channel, the maximum differential voltage of the pins is $\pm 50 \text{mV}$ (35mV rms) |
| 5,6 | IP2, IN2 | Analog input of current channel B, the maximum differential voltage of the pins is $\pm 50 \text{mV}$ (35mV rms) |
| 7 | VP | Voltage signal positive input terminal, maximum differential voltage ± 100 mV (70mV rms) |
| 8 | GND | chip ground |
| 9 | A1 | The address setting pin of the chip, in UART multi-chip |
| 10 | A2 | communication mode, is used to set the address of the chip, |
| 11 | A3 | A4/A3/A2/A1 binary code (0000^1111) , can set the address |
| 12 | A4 | $0^{\sim}15$; inside the pin is Pull-down resistor, if it is |
| | | suspended, it is 0 level, and the pin is directly connected to |
| | | VDD , it is high level . Matches the device address in the UART |
| | | communication protocol |
| 13 | ZX | Voltage zero-crossing indication |
| 14 | I_leak | Leakage/overcurrent alarm output of current B channel |
| 15 | CF | Energy pulse output, see the description of the MODE register for the multiplexing function |



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| 16 | SEL | UART/SPI Communication mode selection (0: UART 1: | | | | | | |
|----|--------|--|--|--|--|--|--|--|
| | | SPI), internal pull- down resistor, | | | | | | |
| | | Floating is O level (UART) , and the pin is directly connected | | | | | | |
| | | to VDD to be high level (SPI) | | | | | | |
| 17 | SCLK | SPI mode clock input; in UART communication mode, it can | | | | | | |
| | | be suspended | | | | | | |
| 18 | RX/SDI | UART/SPI multiplexing pin, UART RX/SPI DIN | | | | | | |
| 19 | TX/SDO | UART/SPI multiplexing pin, UART TX/SPI DOUT, requires an | | | | | | |
| | | external pull-up resistor | | | | | | |
| 20 | VPP | Keep it in the air | | | | | | |



Pin Description (SOP16L)

| pin | symbol | illus | | | | | | |
|------|-------------|--|--|--|--|--|--|--|
| numb | | trat | | | | | | |
| er | | е | | | | | | |
| 1 | VDD | Power supply (+3.3V) | | | | | | |
| 2 | VT | External temperature sensor signal input | | | | | | |
| 3, 4 | IP1, IN1 | Analog input of the current A channel, the maximum differential voltage of the pins is \pm 50mV (35mV rms) | | | | | | |
| 5,6 | IP2, IN2 | Analog input of the current B channel, the maximum differential voltage of the pins is \pm 50mV (35mV rms) | | | | | | |
| 7 | VP | Voltage signal positive input terminal, maximum differential voltage ± 100 mV (70mV rms) | | | | | | |
| 8 | GND | chip ground | | | | | | |
| 9 | ZX | Voltage zero-crossing indication | | | | | | |
| 10 | I_leak | Leakage/overcurrent alarm output of current B channel | | | | | | |
| 11 | CF | Energy pulse output, see the description of the MODE register for the multiplexing function | | | | | | |
| 12 | SEL | UART/SPI Communication mode selection (0: UART 1: SPI), internal pull- down resistor , Floating is 0 level (UART) , and the pin is directly connected to VDD to be high level (SPI) | | | | | | |
| 13 | SCLK | SPI mode clock input, in UART communication mode, just leave it floating | | | | | | |
| 14 | RX/SDI | UART/SPI multiplexing pin, UART RX/SPI DIN | | | | | | |
| 15 | TX/SDO | UART/SPI multiplexing pin, UART TX/SPI DOUT, requires an external pull-up resistor | | | | | | |
| 16 | VPP | Keep it in the air | | | | | | |



1.5 register list

| add ress | name | exter nal read/ | intern al read/ | bit widt | Default s | des crib |
|-------------|-----------------------------|-----------------------|-----------------------|-------------|--------------|---|
| | | write | write | h | | е |
| | | | | Electri | c paramete | er |
| | | | | registe | er (read onl | y) |
| 0x00 | IA_FAST_RMS | R | W | twen | 0x000000 | A channel fast rms, unsigned |
| | | | | ty | | |
| 0.01 | | D | | four | 0.000000 | |
| 0x01 | IA_WAVE | R | W | 20 | 0x000000 | A channel current waveform register, signed |
| 0x02 | IB_WAVE | R | W | 20 | 0x000000 | B channel current waveform |
| | | | | | | register, signed |
| 0x03 | V_WAVE | R | W | 20 | 0x000000 | Voltage waveform register, signed |
| 0x04 | IA_RMS | R | W | twen | 0x000000 | A channel current RMS register, |
| | | | | ty | | unsigned |
| 0.05 | | D | | four | 0.00000 | |
| 0x05 | IB_RMS | R | W | twen | 0x000000 | B channel current RMS register, |
| | | | | ty four | | unsigned |
| 0x06 | V RMS | R | W | twen | 0x000000 | Voltage rms register, unsigned |
| 0,000 | V_NNO | π | " | ty | 0X000000 | vortage rus register, unsigned |
| | | | | four | | |
| 0x07 | IB_FAST_RMS | R | W | twen | 0x000000 | B channel fast rms, unsigned |
| | | | | ty | | |
| | | | | four | | |
| 0x08 | A_WATT | R | W | twen | 0x000000 | A channel active power register, |
| | | | | ty | | signed |
| | | | | four | | |
| 0x09 | B_WATT | R | W | twen | 0x000000 | B channel active power register, |
| | | | | ty four | | signed |
| 0x0A | CFA_CNT | R | W | twen | 0x000000 | A channel active energy pulse |
| UXUA | CI'A_CIVI | K | " | ty | 0x000000 | count, unsigned |
| | | | | four | | |
| 0x0B | CFB_CNT | R | W | twen | 0x000000 | B channel active energy pulse |
| | — | | | ty | | count, unsigned |
| | | | | four | | |
| 0x0C | A_CORNER | R | W | 16 | 0x0000 | A channel current voltage |
| | | | | | | waveform phase angle register |
| 0x0D | B_CORNER | R | W | 16 | 0x0000 | B channel current voltage |
| | | | | | | waveform phase angle register |
| 0x0E | TPS1 Belling Corp., Ltd. | R | W | 10 | 0x000 | Internal temperature detection |

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| | | | | | | register, unsigned | | | | |
|--------|----------------------|-----|---|------------|-----------|--|--|--|--|--|
| 0x0F | TPS2 | R | W | 10 | 0x000 | External temperature detection register, unsigned | | | | |
| | I | | | User | operation | | | | | |
| | register (read and | | | | | | | | | |
| write) | | | | | | | | | | |
| 0x10 | IA_FAST_RMS _CTRL | R/W | R | 16 | 0xFFFF | A channel fast rms control register | | | | |
| 0x13 | IA_RMSOS | R/W | R | 8 | 0x00 | Current A channel RMS small signal correction register | | | | |
| 0x14 | IB_RMSOS | R/W | R | 8 | 0x00 | Current B channel RMS small signal correction register | | | | |
| 0x15 | A_WATTOS | R/W | R | 8 | 0x00 | A channel active power small signal correction register | | | | |
| 0x16 | B_WATTOS | R/W | R | 8 | 0x00 | B channel active power small signal correction register | | | | |
| 0x17 | WA_CREEP | R/W | R | 8 | 0x0B | Active power anti-passage register | | | | |
| 0x18 | MODE | R/W | R | 16 | 0x0000 | User Mode Select Register | | | | |
| 0x19 | SOFT_RESET | R/W | R | twen | 0x000000 | When writing Ox5A5A5A, the user | | | | |
| | | | | ty four | | area register is reset | | | | |
| Ox1A | USR_WRPROT | R/W | R | 8 | 0x00 | User write-protect setting register. After writing 0x55 , use The user operation register can be written; write other values, | | | | |
| | | | | | | the user operation register area cannot be written | | | | |
| 0x1B | TPS_CTRL | R/W | R | 16 | 0x07FF | Temperature Mode Control Register | | | | |
| 0x1C | TPS2_A | R/W | R | 8 | 0x0000 | External Temperature Sensor Gain Coefficient Correction Register | | | | |
| 0x1D | TPS2_B | R/W | R | 8 | 0x0000 | External Temperature Sensor Offset Coefficient Correction Register | | | | |
| Ox1E | IB_FAST_RMS _CTRL | R/W | R | 16 | 0xFFFF | B channel fast rms control register | | | | |



1.6 Special Register Description

1.6.1 User Mode Select Register

| 0x18 | MODE | | Operating Mode Register | | | |
|---------|----------------|---------------|--|---|--|--|
| No. | name | default value | otion | | | |
| [7:0] | reserved | 0b0000000 | reser | rve | | |
| 8 | RMS_UPDATE_SEL | 0b0 | RMS register refresh time selection choose | 0: 400ms 1: 800ms | | |
| 9 | AC_FREQ_SEL | 0b0 | AC frequency selection | 0: 50Hz 1: 60Hz | | |
| 10 | reserved | 0b0 | reserve | | | |
| 11 | CF_SEL | 0b0 | CF pin output energy pulse selection | 0: A channel 1: B channel | | |
| 12 | CF_UNABLE | 0Ь0 | CF pin output function selection | 0: energy pulse, MODE[11] The configuration is valid 1: alarm function, TPS_CTRL[14] is configured with effect | | |
| [15:13] | reserved | 0b000 | reser | rve | | |



1.6.2 Temperature Mode Control Register

| 0x1B | TPS_CTRL | Temperature Mod | le Control Register | |
|------|----------|-----------------|--|--|
| No. | name | default value | description | |
| | | | [15] Temperature measurement switch, default ObO, open Start measuring temperature | 0: open 1: off |
| 0x1B | TPS_CTRL | 0x07FF | [14] Alarm switch, default ObO, | 0: Temperature alarm is on 1 : Current A channel overcurrent / leakage report alarm on |
| | | | [13:12] Temperature measurement selection, default Ob00 automatic temperature measurement | 00: automatic temperature measurement 01: Same as 00 10: Internal temperature measurement 11: External temperature measurement |
| | | | <pre>[11:10] Temperature measurement time interval selection, default 0b01 100ms [9:0] External temperature measurement alarm threshold setting Set, the default setting is 0x3FF, no alarm</pre> | 00: 50ms 01: 100ms 10: 200ms 11: 400ms The TPS2 register value is greater than or equal to the report Alarm value, generate an alarm |



1.7 Performance

1.7.1 Electrical parameter performance

(VDD = 3.3V, GND = 0V, on-chip reference voltage source, built-in crystal oscillator, 25 °C, electric energy is measured through CF output)

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| symbol | Measuremen t conditions | the smalles t | typical | max imu m | unit |
|--------|--|--|---|--|---|
| VDD | | 3.0 | | 3.6 | V |
| Iop | VDD=3.3V | | 3 | | mA |
| | 4000:1 input drive state range | | | | |
| | 35A~100mA output Into @ 1mohm sampling resistor | | 0.2 | | % |
| | 100mA [~] 50mA input@lmohm sampling resistance | | 0.4 | | % |
| | 50mA~10mA input Into @ 1mohm sampling resistor | | 0.6 | | % |
| | 35A~100mA input@1mohm sampling resistance | | 0.2 | | % |
| | 100mA~50mA input@lmohm sampling resistance | | 2 | | % |
| FOIL | 50mA~10mA input@1mohm sampling resistance | 10 | 6 | 10 | % M |
| | VDD | VDDVDDIopVDD=3. 3V4000:1 input drive state range35A~100mA outputInto @ 1mohm sampling resistor100mA~50mA input @ 1mohm sampling resistance50mA~10mA inputInto @ 1mohm sampling resistance50mA~10mA inputInto @ 1mohm sampling resistance100mA~50mA input @ 1mohm sampling resistor100mA~50mA inputInto @ 1mohm sampling resistor100mA~10mA input input @ 1mohm sampling resistance100mA~50mA input @ 1mohm sampling resistance100mA~50mA input @ 1mohm sampling resistance50mA~10mA input @ 1mohm sampling resistance50mA~10mA input @ 1mohm sampling resistance50mA~10mA input @ 1mohm sampling resistance50mA~10mA input @ 1mohm sampling resistance | t conditionssmalles tVDD3.0IopVDD=3.3V4000:1 input drive4000:1state range35Å~100mAoutput1Into @ 1mohm sampling resistor100mA~50mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistor100mA~50mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance50mA~10mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance50mA~10mAinput @ 1mohm sampling resistance100mA~50mAinput @ 1mohm sampling resistance50mA~10mAinput @ 1mohm sampling resistance50mA~10mA< | t conditionssmalles tVDD3.0IopVDD=3.3V4000:1 input drive34000:1 input drive34000:1 input drive0.2state range0.2Into @ 1mohm sampling resistor0.2Into @ 1mohm sampling resistor0.4Sampling resistance0.4Sampling resistance0.4Sampling resistance0.6Into @ 1mohm sampling resistance0.6Into @ 1mohm sampling resistance0.6Into @ 1mohm sampling resistance0.250mA^10mA input @ 1mohm input @ 1mohm0.235A^100mA input @ 1mohm0.2sampling resistance0.2Sampling resistance2Sampling resistance2Sampling resistance2Sampling resistance2Sampling resistance6Sampling resistance6Sampling resistance6 | t conditionssmalles timu mVDD3.03.6IopVDD=3.3V34000:1 input drive34000:1 input drivestate range35Å~100mA output0.2Into @ 1mohm sampling resistor0.2Into @ 1mohm sampling resistor0.4100mA~50mA input @ 1mohm sampling resistance0.450mA~10mA input0.6Into @ 1mohm sampling resistance0.6100mA~50mA input0.6100mA~50mA input0.6100mA~50mA input0.235A~100mA input0.2100mA~50mA input @ 1mohm sampling resistance0.235A~100mA input @ 1mohm sampling resistance0.250mA~10mA input @ 1mohm input @ 1mohm0.250mA~10mA input @ 1mohm sampling resistance250mA~10mA input @ 1mohm sampling resistance250mA~10mA input @ 1mohm sampling resistance650mA~10mA input @ 1mohm resistance6 |

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| 1 | time | 60Hz | cycle/ | 8.3 | | 33 | М |
|----|---|---------|------------------------------|-----|-----|-----|---|
| | | | half cycle | | | | |
| Ze | ero-crossing signal output delay | | | | 571 | | u |
| (| The phase angle between channels causes measurement errors | PF08err | Phase lead 37 (PF=0.8) | | | 0.5 | % |
| | Poor (capacitive) | | | | | | |
| C | The phase angle between channels causes measurement | PF05err | Phase lag 60 (PF=0.5) | | | 0.5 | % |
| F | errors Poor (sensibility) | | | | | | |
| | AC Power Supply Rejection (Output Frequency | ACPSRR | IP/N=100mV | | | 0.1 | % |
| | rate amplitude change) | | | | | | |
| D | C supply rejection (output frequency | DCPSRR | VP/N=100mV | | | 0.1 | % |
| | rate amplitude change) | | | | | | |





| Measurement items | symbol | Measuremen t conditions | the smalles t | typical | max imu m | unit |
|---------------------------------|--------|--|---------------------|---------|-----------------|------|
| Analog input level (current) | | Current differential input (peak) | | | 50 | mV |
| Analog input level (voltage) | | Voltage differential input (peak) | | | 200 | mV |
| Analog input impedance | | | | 370 | | kΩ |
| SEL pull-down resistor | | SEL (pull down) | | 56.9 | | kΩ |
| Analog input bandwidth | | (-3dB) | | 3.5 | | kHz |
| Internal Voltage Reference | Vref | | | 1.218 | | V |
| logic input high | | VDD=3. $3V \pm 5\%$ | 2.6 | | | V |
| Logic input low | | VDD=3. $3V \pm 5\%$ | | | 0.8 | V |
| logic output high | | VDD=3.3V±5% IOH=5mA | VDD-0.5 | | | V |
| Logic output low level | | VDD=3.3V±5% IOL=5mA | | | 0.5 | V |

1.7.2 limit range

(**T = 25** ° C)

| project | symbol | extremum | unit |
|---|---|------------------------|------|
| Power supply voltage VDD | VDD | -0.3 ~ +4 | V |
| Analog input voltage (relative to GND) | IP1, IP2, VP | $-4 \sim +4$ | V |
| Digital input voltage (relative to GND) | A1 [~] A4, UART_SEL, RX/SDI | -0.3 ~ VDD+0.3 | V |
| Digital output voltage (relative to GND) | CF, I_Leak, TX/SDO | -0.3 ~ VDD+0.3 | V |
| Operating temperature | Topr | -40 $^{\sim}$ $+105$ | °C |
| storage temperature | Tstr | -55 $^{\sim}$ $+150$ | °C |



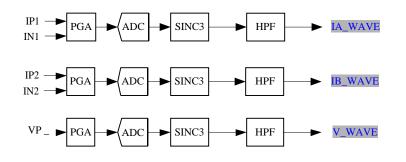
2 Functional description

BL0939 is mainly divided into analog signal processing and digital signal processing. The analog part mainly includes three-channel PGA, three-channel Sigma-Delta ADC, built-in clock (internal clock), power on/reset monitoring (Power on/reset), temperature detection (temperature

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sensor), LDO and other related analog modules, and the digital part is a digital signal
processing module (DSP).

2.1 Current and voltage transient waveform measurement





As shown in the figure above, two channels of current and one channel of voltage pass through the analog module amplifier (PGA) and high-precision analog-to-digital conversion (ADC) respectively to obtain three channels of 1bit PDM for the digital module, and the digital module passes through the down-sampling filter (SINC3), Qualcomm Filter (HPF), channel offset correction and other modules to obtain the required current waveform data and voltage waveform data (IA_WAVE, IB_WAVE, V_WAVE).

BL0939 has three high-precision ADCs, and the current adopts double-ended differential signal input: A current channel IP1/IN1, B current channel IP2/IN2, voltage channel VP.

The collected load current and voltage waveform data are updated at a rate of 7.8k, and each sampled data is a 24bit signed number, which is stored in the waveform register (IA_WAVE, IB_WAVE, V_WAVE) respectively, and the SPI rate configuration is greater than 375Kbps, which



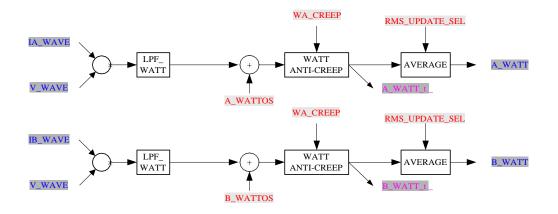
can be read continuously Waveform value for one channel.

Note: The register is **24bit**, if the number of digits is insufficient, the high bits are filled with zeros;

| addre ss | name | exter nal read/ write | intern al read/w rite | bit width | Defaults | describe |
|-------------|---------|--------------------------------|--------------------------------|--------------------|----------|--|
| 0x01 | IA_WAVE | R | W | twen ty four | 0x000000 | A channel current waveform register |
| 0x02 | IB_WAVE | R | W | twen ty four | 0x000000 | B channel current waveform register |
| 0x03 | V_WAVE | R | W | twen ty four | 0x000000 | Voltage Waveform Register |



2.2 active power





| addre ss | name | extern al read/w rite | intern al read/w rite | bit width | Defaults | describe |
|-------------|--|--------------------------------|--------------------------------|--------------------|---|---------------------------|
| 0x08 | A_WATT | R | W | twen ty four | 0x000000 | A channel active register |
| 0x09 | B_WATT | R | W | twen ty four | 0x000000 | B channel active register |
| - | Active power calculation formula : A/B_WATT = | | | | A) *V(V) os(φ) ref ² | |

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Among them, I(A), V(V) is the effective value (mV) of the channel pin input signal, φ is the phase angle of the I(A) and V(V) AC signals, Vref is the built-in reference voltage, typical value is 1.218V.

These two registers indicate whether the current active power is positive work or negative work, Bit[23] is the sign bit, Bit[23]=0, the current power is positive work, Bit[23]=1, the current power is negative work, in complement form.

2.3 Active Power Offset Calibration

 $BL0939 \mbox{ contains two 8 -bit active power offset correction registers (A_WATTOS , B_WATTOS), the default value is 00H . They use the data in 2 's complement form to eliminate the deviation of active power when measuring electric energy, and Bit[7] is the sign bit. The Shanghai Belling Corp., Ltd. 20/35$



deviation here may be due to board-level noise or crosstalk. Offset correction can make the value in the active power register close to 0 at no load .

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| addre ss | name | extern al read/w rite | inter nal read/ write | bit width | Default s | describe |
|-------------|----------|--------------------------------|--------------------------------|--------------|--------------|--|
| 0x15 | A_WATTOS | R/W | R | 8 | 0x00 | A channel power small signal correction register |
| 0x16 | B_WATTOS | R/W | R | 8 | 0x00 | B channel power small signal correction register |

$WATTOS = \frac{WATT - WATT0}{8 \times 3.05172}$

 WATT is the active power after correction, and $\mathsf{WATT0}$ is the active power before correction.





2.4 Active power anti-creep

BL0939 has a patented power anti-submersion function, which ensures that the board-level noise power will not accumulate power when there is no current input.

BL0939

active anti-creep threshold register (WA_CREEP), is an 8bit unsigned number, and the default is OBH. The corresponding relationship between this value and the active power register value is shown in the following formula. When the absolute value of the input active power signal is less than this value, the output active power is set to O. This can make the value output to the active power register be O in the case of no load, even if there is a small noise signal, and the electric energy will not accumulate.

| addre ss | name | extern al read/w rite | inter nal read/ write | bit width | Default s | describe |
|-------------|----------|--------------------------------|--------------------------------|--------------|--------------|---------------------------------------|
| 0x17 | WA_CREEP | R/W | R | 8 | 0x0B | Active power anti-passage register |

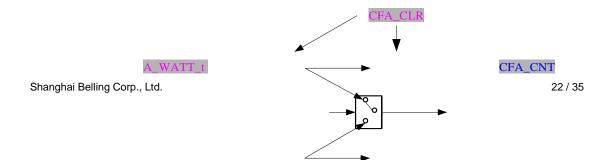
set according to the value of the power register $A_WATT/B_WATT, and$ their corresponding relationship

 $WA_CREEP = \frac{WATT}{3.0517578125*8}$

Note: When the channel is in the anti-submarine state, the effective value of the current of the channel is not measured, and it is also cut to **0**.

2.5 Energy Metering

BL0939 provides two-channel energy pulse metering. The active instantaneous power of the two channels is integrated according to time to obtain active energy, and the calibration pulse CF is output in proportion . The CFA_CNT and CFB_CNT registers store the number of output energy pulse CF, as shown in the figure below Show.



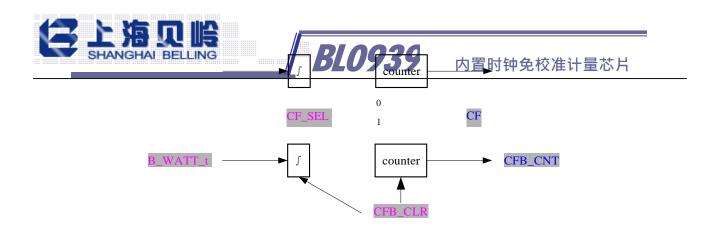


Figure 6



| 0x18 | MODE | Operating Mode Register | | | | | |
|------|-----------|----------------------------|--|---|--|--|--|
| No. | name | default value | description | | | | |
| 10 | reserved | 0b0 | res | erve | | | |
| 11 | CF_SEL | 0b0 | CF pin output energy pulse pass Road selection | 0: A channel 1: B channel | | | |
| 12 | CF_UNABLE | 0b0 | CF pin output selection | <pre>0: Energy pulse MODE[11] configuration is valid 1: Temperature measurement/leakage</pre> | | | |
| | | | | alarm TPS[14] configuration is valid | | | |

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First set MODE[12]=0 to select the CF pin to output energy pulse, and then set MODE[11] to choose to output the energy pulse of channel A or channel B.

| addre | name | exter nal | intern al | bit | Defaults | describe |
|-------|---------|----------------|----------------|-------|----------|-------------------------------|
| SS | | read/ write | read/w rite | width | | |
| OxOA | CFA_CNT | R | W | twen | 0x000000 | A channel active energy pulse |
| | | | | ty | | count, unsigned |
| | | | | four | | |
| 0x0B | CFB_CNT | R | W | twen | 0x000000 | B channel active energy pulse |
| | | | | ty | | count, unsigned |
| | | | | four | | |

The counting of active energy pulses is applied to the applied energy, and the results are stored in two registers, CFA_CNT and CFB_CNT, and can also be accessed through I/O interrupt directly counts the number of pulses from the CF pin. When the period of CF is less than 180ms, it is a pulse with a 50% duty cycle, which is greater than or equal to 180ms, the high level fixed pulse width is 90ms.

Note: CFA_CNT and CFB_CNT registers are the algebraic and

accumulation methods of electric energy pulses, that is, positive power

is added and negative power is subtracted.



The accumulation time for each CF pulse $t_{\mbox{ CF}}$ =

Where WATT is the corresponding active power register value (A_WATT, B_WATT).

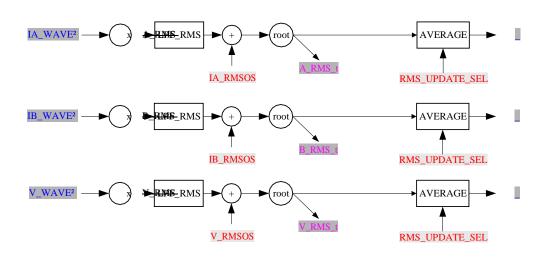
BL0939

2.6 RMS value of current and voltage

WATT

The effective value of the three channels, as shown in the figure below, passes through the square circuit (X^2), low-pass filter (LPF_RMS), and root circuit (ROOT) to obtain the instantaneous value RMS_t of the effective value, and then obtains the average of the three channels by averaging values (A_RMS, B_RMS, and V_RMS).





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Figure 7

| addre ss | name | extern al read/w rite | intern al read/w rite | bit width | Defaults | describe |
|-------------|--------|--------------------------------|--------------------------------|--------------------|----------|---|
| 0x04 | IA_RMS | R | W | twen ty four | 0x000000 | A channel current RMS register, unsigned |
| 0x05 | IB_RMS | R | W | twen ty four | 0x000000 | B channel current RMS register, unsigned |
| 0x06 | V_RMS | R | W | twen ty four | 0x000000 | Voltage rms register, unsigned |

| 0x18 | MODE | Operating Mode Register | | | | | |
|------|----------------|------------------------------|----------------------------|----------------------|--|--|--|
| No. | name | default value description | | | | | |
| 8 | RMS_UPDATE_SEL | 0b0 | RMS update speed selection | 0: 400ms 1: 800ms | | | |

Set MODE[8].RMS_UPDAT_SEL, you can choose the average refresh time of the effective value to be 400ms or 800ms, and the default is 400ms. When a current channel is in the anti-submarine state, the effective value of the current channel is zero.

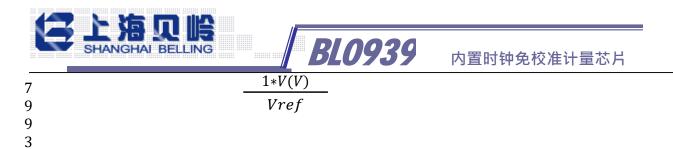
324004 * I(A)

Vref

Current RMS conversion formula: IA/B_RMS =

Voltage RMS conversion formula: V_RMS =

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 Vref is the reference voltage, the typical value is 1.218V.

Note: I(A) is the input signal (mV) between IP1 and IN1 pins , V(V) is the input signal (mV) of VP pin .



2.7 Current Voltage RMS Offset Calibration

BL0939 contains two 8 -bit RMS offset registers (IA_RMSOS and IB_RMSOS), their default value is OOH , and they use 2 's complement code form data to adjust the deviation in RMS calculation. This deviation may come from input noise. Offset correction can make the value in the rms register close to Oatnoload.

BL0939

| addre ss | name | extern al read/w rite | inter nal read/ write | bit width | Default s | describe |
|-------------|----------|--------------------------------|--------------------------------|--------------|--------------|-----------------------------|
| 0x13 | IA_RMSOS | R/W | R | 8 | 0x00 | IA current RMS small signal |
| | | | | | | correction register |
| 0x14 | IB_RMSOS | R/W | R | 8 | 0x00 | IB Current RMS Small Signal |
| | | | | | | Correction Register |

Calibration formula $\frac{RMSOS}{9.3132 \times 2^{15}} = \frac{RMS^2 - RMSO^2}{2}$

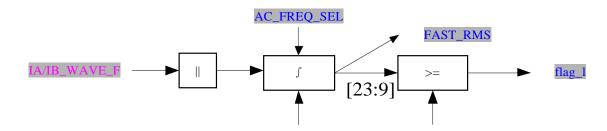
Here $\mathsf{RMSO}\,\mathsf{is}$ the effective value before correction, and $\mathsf{RMS}\,\mathsf{is}$ the effective value after correction.

2.8 Leakage / overcurrent detection

and B of BL0939 have fast RMS registers, which can detect half cycle or cycle RMS. This function can be used for leakage or overcurrent detection. For the source of the leakage waveform I_WAVE , refer to the channel waveform block diagram. After taking the absolute value of IA/IB_WAVE_F , the half cycle or cycle time is accumulated, which is selected by FAST_RMS_CTRL[15]. The default value is 1 to select cycle accumulation, and the response time is up to 40ms (50Hz) or 33mS

(60Hz), note that the jump of the x_FAST_RMS register is relatively large when the half cycle is accumulated . To distinguish the half cycle time of 50Hz and 60Hz

(AC_FREQ_SEL).



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[15]

内置时钟免校准计量芯片

FAST_RMS_CTRL [14:0]

Figure 8



BL0939 内置时钟免校准计量芯片

| addre ss | name | extern al read/w rite | inter nal read/ write | bit width | Default s | desc ribe |
|-------------|------------------|--------------------------------|--------------------------------|--------------|--------------|----------------------------|
| 0x10 | IA_FAST_RMS_CTRL | R/W | R | 16 | 0xFFFF | A channel fast rms control |
| | | | | | | register |
| Ox1E | IB_FAST_RMS_CTRL | R/W | R | 16 | 0xFFFF | B channel fast rms control |
| | | | | | | register |

Through two fast RMS control registers, $IA_FAST_RMS_CTRL$ and $IB_FAST_RMS_CTRL$, the refresh time can be selected as half cycle or cycle, and the fast RMS threshold (that is, leakage or overcurrent threshold) can be set .

| | | Channel Fast RMS Register | | | | |
|------|------------------|------------------------------|--|---------------------------|--|--|
| No. | name | default value description | | | | |
| 0x10 | IA_FAST_RMS_CTRL | 0xFFFF | [15] A channel fast RMS register refresh time [14:0] A channel fast RMS threshold | 0: half cycle 1: Cycle | | |
| 0x1E | IB_FAST_RMS_CTRL | OxFFFF | [15] B channel fast RMS register refresh time [14:0] B channel fast RMS threshold | 0: half cycle 1: Cycle | | |

| 0x18 | MODE | Operating Mode | | | | |
|------|-------------|------------------------------|------------------------|---------|--|--|
| | | Register | | | | |
| No. | name | default value description | | | | |
| 9 | AC EDEO CEL | 0b0 | AC frequency coloction | 0: 50Hz | | |
| 9 | AC_FREQ_SEL | 000 | AC frequency selection | 1: 60Hz | | |

Set AC frequency by $\ensuremath{\mathsf{MODE[9]}}$.

| addre | name | exter nal | inter nal | bit wid | Defaults | describe |
|-------|-------------|--------------|--------------|------------|----------|---------------------|
| SS | | read/ | read/ | th | | |
| | | write | write | | | |
| 0x00 | IA_FAST_RMS | R | W | tw | 0x000000 | A channel fast rms, |
| | | | | en | | unsigned |
| | | | | ty | | |
| | | | | fo | | |
| | | | | ur | | |
| 0x07 | IB_FAST_RMS | R | W | tw | 0x000000 | B channel fast rms, |
| | | | | en | | unsigned |

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| | DIADO | 内置时钟免校准计量芯片 | |
|--|-------|-------------|--|
| | ty | | |
| | fo | | |
| | ur | | |

24 -bit unsigned fast effective value register according to the cycle or half cycle , compare Bit[23:9] of the FAST_RMS register with the leakage / overcurrent threshold FAST_RMS_CTRL [14:0] , if it is greater than or equal to the set threshold, the leakage / Overcurrent alarm output indicates that the pin outputs a high level.

 $B\ leakage\ /\ overcurrent\ alarm\ output\ indication\ pin\ is\ I_leak$, which can be output directly without configuration.

leakage /overcurrent alarm output indication pin of channel $A\,is\,CF\,,$ you need to set $MODE[12]{=}1\,first\,,$ and then set <code>TPS_CTRL[14]=1.</code>

| 0x18 | MODE | Operating Mode Register | | | | |
|------|-----------|----------------------------|----------------------------|---|--|--|
| No. | name | default value | | | | |
| 12 | CF_UNABLE | 0b0 | CF pin output selection | 0: Energy pulse MODE[11] configuration is valid 1: Temperature measurement/leakage alarm TPS[14] configuration is valid | | |



| 0x1B | TPS_CTRL | Temperature Mode | | | | |
|------|------------|---------------------------|-----------------|---|--|--|
| | | Control Register | | | | |
| No. | name | default value description | | | | |
| | | | | 0: Temperature alarm is on | | |
| 14 | ALERT_CTRL | 0b0 | alarm switch | 1: Current A channel overcurrent/leakage alarm is on | | |

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Since the fast effective value is updated by cycle or half cycle, the response time of $I_{\text{leak is up to 2}}$ cycles or 2 half cycles.

2.9 Phase angle calculation

BL0939 can be used for phase angle measurement, and the phase angle CORNER_A/CORNER_B between A/B two-phase current and voltage indicates the reactive quadrant. The calculation is obtained by the positive zero-crossing time difference of the current and the voltage. When the current is positively zero-crossing, it is updated to the register CORNER_A/CORNER_B, and each register is a 16-bit unsigned number.

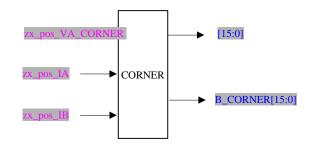


Figure 9

| addre ss | name | extern al read/w rite | inter nal read/ write | bit width | Default s | describe |
|-------------|----------|--------------------------------|--------------------------------|--------------|--------------|--|
| 0x0C | A_CORNER | R | W | 16 | 0x0000 | A channel current voltage waveform phase angle register |
| 0x0D | B_CORNER | R | W | 16 | 0x0000 | B channel current voltage waveform phase angle register |

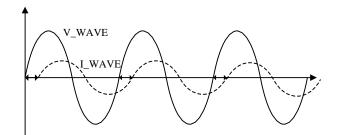




Figure 10

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Phase angle conversion formula: unit is radian $2*pi*A/B_CORNER* f_c f_0$

Among them , f_c is the measurement frequency of the AC signal source, the default is 50Hz, f_0 is the sampling frequency, the typical value is 1MHz.



2.10 Zero-crossing detection

BL0939 provides voltage zero-crossing detection, and the zero-crossing signal is directly output from the pin ZX.ZX is 0, which means the positive half cycle of the waveform, and ZX is 1, which means the negative half cycle of the waveform. The time delay with the actual input signal is 570us.

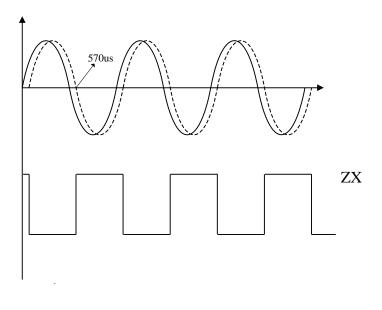


Figure 11



2.11 Thermometer

BL0939 provides internal temperature measurement and off-chip temperature measurement.

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When the external temperature is measured, the optional output alarm indication, when the alarm function is turned on, the CF pin can be reused as an output alarm signal, when TPS2 is greater than or equal to the alarm threshold, the CF pin outputs a high level, and the temperature indication alarm. When the temperature value is lower than the alarm value or the alarm function is turned off, the alarm indication will be exited.

| 0x1B | TPS_CTRL | Temperature Mode Control Register | | | | | |
|------|----------|--------------------------------------|--|---|--|--|--|
| No. | name | default value | on | | | | |
| | | | [15] Temperature measurement switch, default ObO, open Start measur ing temper ature | 0: open 1: off | | | |
| 0x1B | TPS_CTRL | 0x07FF | [14] Alarm switch, default ObO, | 0: Temperature alarm is on 1: Current A channel overcurrent / Leakage alarm on | | | |
| | | | [13:12] Temperature measurement selection, default ObOO automatic temperature measurement | 00: automatic temperature measurement 01: Same as 00 10: Internal temperature measurement 11: External temperature measurement | | | |
| | | | <pre>[11:10] Temperature measurement time interval selection, default 0b01 100ms [9:0] External temperature measurement alarm threshold setting</pre> | 00: 50ms 01: 100ms 10: 200ms 11: 400ms | | | |



set, the default setting is 0x3FF

First set MODE[12]=1, and then set TPS_CTRL[14]=0, the CF pin can be turned on to output an external temperature alarm indicator.

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| 0x18 | MODE | Operating Mode | | | | | |
|------|-----------|----------------|----------------------------|--|--|--|--|
| | | | Register | | | | |
| No. | name | default value | default value description | | | | |
| 12 | CF_UNABLE | 0b0 | CF pin output selection | <pre>0: Energy pulse MODE[11] configuration is valid 1: Temperature measurement alarm TPS[14] configuration is valid</pre> | | | |

External and internal temperature readings are stored in two registers, $\ensuremath{\mathsf{TPS1}}$ and $\ensuremath{\mathsf{TPS2}}$, respectively.

| addre ss | name | extern al | nal | bit width | Default s | describe |
|-------------|------|--------------|-------|--------------|--------------|--------------------------|
| ~~ | | read/w | read/ | | ~ | |
| | | rite | write | | | |
| 0x0E | TPS1 | R | W | 10 | 0x0000 | Internal temperature |
| | | | | | | value register, unsigned |
| 0x0F | TPS2 | R | W | 10 | 0x0000 | External temperature |
| | | | | | | value register, unsigned |



Internal temperature measurement formula: Tx=(170/448)(TB/2-32)-45

TB is the TPS1 register value;

The external test temperature adopts SAR ADC, the maximum input signal of VT pin is 0.55*VDD (V), and the value of TPS2 register is the corresponding AD

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sampled value, full scale $1024\,,$

| addre ss | name | extern al read/w rite | intern al read/w rite | bit width | Default s | describe |
|-------------|--------|--------------------------------|--------------------------------|--------------|--------------|---|
| 0x1C | TPS2_A | R/W | R | 8 | 0x00 | External Temperature Sensor Gain Coefficient A Correction Register |
| Ox1D | TPS2_B | R/W | R | 8 | 0x00 | External Temperature Sensor Bias Coefficient B Correction Register |



3 Communication Interface

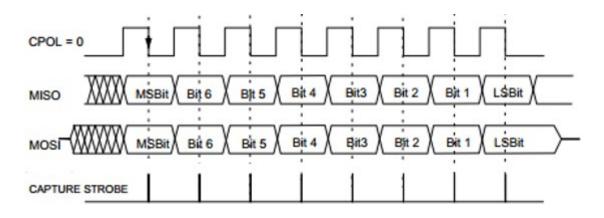
register data is sent in 3 bytes (24bit). For the register data less than 3 bytes, the unused bits are filled with 0, and 3 bytes are sent.

3.1 SPI

- Through the pin UART_SEL choose , with UART reuse
- ●●●����� mode
- \bullet $$\rm Half-duplex\ communication$, the communication rate can be configured , the maximum communication rate 900khz
- 8-bit data transfer, MSB First , LSB is behind
- ●☞光⊠ a clock polarity / phase (CPOL=0, CPHA=1)

3.1.1 Operating mode

The master device works in Mode1: CPOL=0, CPHA=1, that is, in the idle state, SCLK is at low level, and data transmission is at the first edge, that is, the transition of SCLK from low level to high level, So data sampling is on the falling edge, and data transmission is on the rising edge.





3.1.2 frame structure

In communication mode, first send 8bit identification byte (0x55) or (0xA5), (0x55) is the identification byte for read operation, (0xA5) is the identification byte for write



operation , and then send the register address byte to decide to access the register address (see BL0939 Register List) . The figure below shows the data transfer sequence for read and write operations, respectively. After one frame of data transmission is completed, BL0939 re-enters the communication mode. The number of SCLK pulses required for each read / write operation is 48 bits.

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There are two frame structures, which are described as follows:



1) Write operation frame

| write frame OxA5 | ADDR[7:0] | DATA_H[7:0] | DATA_M[7:0] | DATA_L[7:0] | CHECKSUM[7:0] | |
|------------------|-----------|-------------|-------------|-------------|---------------|--|
|------------------|-----------|-------------|-------------|-------------|---------------|--|

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Among them, the checksum byte CHECKSUM $\dot{s}((OxA5 + ADDR + DATA_H + DATA_M + DATA_L) & OxFF)$ and then reversed bit by bit.

2) Read operation frame



return data

| DATA | _H[7:0] | DATA_M[7:0] | DATA_L[7:0] | CHECKSUM[7:0] | |
|------|---------|-------------|-------------|---------------|--|
|------|---------|-------------|-------------|---------------|--|

Among them, the checksum byte CHECKSUM is((0x55+ADDR+DATA_H+DATA_M+DATA_L) & OxFF) and then reversed bit by bit. Note: The data is a fixed 3 bytes (the high byte is in front, the low byte is in the back, if the data valid byte is less than 3 bytes, the invalid bit is filled with 0)

3.1.3 Write Operation Timing

The serial write sequence is performed as follows. The frame identification byte {OxA5} indicates that the data communication operation is to write data, and ADDR is the address of the register that needs to write data. The MCU will prepare the data bits that need to be written into BL0939 before the falling edge of SCLK, and start shifting in the register data at the falling edge of the clock of SCLK. All remaining bits of the register data are also shifted left on the falling edge of this SCLK (Fig. 13).

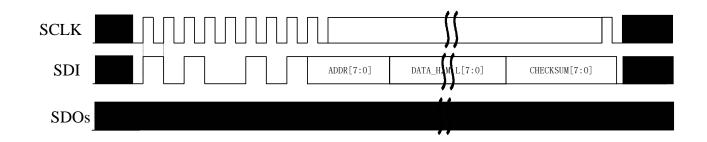






Figure 13

3.1.4 Read Operation Timing

During the data read operation of BL0939 , on the rising edge of SCLK , BL0939 outputs the corresponding data bit to the SDO logic output pin, and the SDO value remains unchanged during the next SCLK is 1 , that is, in the next On the falling edge, an external device can sample the SDO value. During the data read operation, the MCU must first send a read command frame.

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|-------|------------------------------|
| SCLK | |
| SDOs | DATA_H,ML[7:0] CHECKSUM[7:0] |



When BL0939 is in the communication mode, the frame identification byte {0x55} indicates
that the data communication operation is read data. followed by the bytes
ADDR is the address of the target register to be read. After the BL0939 receives the register
address, it starts to shift out the data in the register on the rising edge of SCLK (Figure 14).
All remaining bits of the register data are shifted out on subsequent SCLK rising edges.
Therefore, on the falling edge of SCLK, the external device can sample the output data of SPI.
Once the read operation is complete, the serial interface re-enters communication mode. At
this time,

SDO output goes into a high-impedance state on the falling edge of the last SCLK signal.

3.1.5 SPI Interface fault tolerance mechanism

1) The soft reset function of the SPI interface can reset the SPI interface independently by sending 6 bytes of 0xFF through the SPI interface.

Note: SPI communication does not support chip selection. If you choose a 20pin package, you need to connect A4A2 to ground and A3A1 to high level.



3.2 UART

3.2.1 overview

BL0939 can use UART communication. The UART interface only needs two low-

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speed optocouplers to realize isolated communication. Fixed baud rate

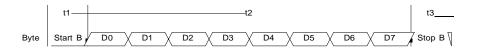
4800bps, N, 8, 1.5, working in slave mode, half-duplex communication.

Both packages have UART communication, and the 20 pin package has a chip select address [A4 A3 A2 A1], and the device address 00~15 can be set.

3.2.2 describe

UART port settings: communication baud rate 4800bps, no parity, stop bit 1.5.

3.2.3 format per byte



Start bit low level duration t1=208us

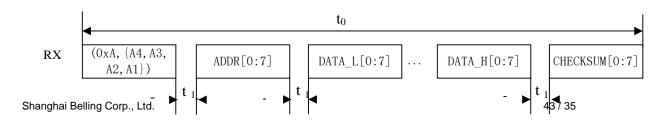
Valid data bit time lasts t2=208*8=1664us

Stop bit high level duration t3=208us+104us

3.2.4 write timing

host UART write data sequence is shown in the figure below. The host first sends the command byte (OxA,{A4,A3,A2,A1}), and then needs to write the data register address (ADDR), and then sends the data byte (The low byte is in front, the high byte is in the back, and the valid data bytes are insufficient

 $\mathbf 3$ byte, invalid bits are filled with $\mathbf 0\,)$, and finally the checksum byte.







 $(0 \times A, \{A4, A3, A2, A1\})$ is the frame identification byte of the write operation, if [A4A1]=0101, the device address is 5, and the frame identification byte is 0xA5.

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ADDR is the internal register address of BL0939 corresponding to the write operation . The CHECKSUM byte is (((OxA,{A4,A3,A2,A1})+ADDR+Data_L+Data_M+Data_H) & OxFF) and then reversed bit by bit. Note: The device address of BL0939-SOP16L is 5, that is, the first byte is OxA5.

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3.2.5 read timing

host UART read data sequence is shown in the figure below, the host first sends the command byte $(0x5, \{A4, A3, A2, A1\})$, then sends the register address (ADDR) to be read, and then BL0939 sends the data byte in turn (The low byte is in front, the high byte is in the back, if the data valid byte is less than 3 bytes, the invalid bit is filled with 0), and the last checksum byte.



 $(0 \times 5, \{A4, A3, A2, A1\})$ is the frame identification byte of the read operation; if [A4A1] = 0101, the device address 5, the frame identification byte is 0×55 ; ADDR is the internal register address of BL0939 corresponding to the read operation; CHECKSUM The byte is

(((Ox5,{A4,A3,A2,A1})+ADDR+Data_L+Data_M+Data_H) & OxFF) and then reversed bit by bit;

Timing description

| | illustrate | Min | type | Max | unit |
|----|--|-----|------|-----|------|
| t1 | Interval time between MCU sending bytes | 0 | | 20 | М |
| t2 | Interval time from the end of MCU sending register address to BL0939 sending byte during read operation | | 72 | | u |



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| t3 | Interframe time | 0.5 | | u | |
|----|---|-----|-----|---|--|
| t4 | Interval time between bytes sent by BL0939 | | 116 | u | |



3.2.6 packet sending mode

Through the command " (0x5,{A4,A3,A2,A1}) + 0xAA", BL0939 will return a full power parameter packet. A total of 35 packets were returned

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bytes, 4800 bp s time cost 77 m s. The specific format is: Baotou (1 byte h ead → M ◆ □□ M ■ ◆ _ A Fast RMS (3 byte IA_FAST_RMS)

→ Current A RMS value (3byte IA_RMS) → Current B RMS value (3byte IB_RMS) → Voltage RMS value (3byte V_RMS) →

electric current B Fast RMS (3 b y t e IB_F A ST_R M S)→ A Channel power value (3 byte A_W A TT)→ B Channel power value (3 byte B_WATT) __

| name | byte order | content | name | byte order | content |
|-------------|---------------|---------------|----------|---------------|-----------|
| | No | | | No | |
| Baot | 0 | Head (0x55) | | 19 | B_WATT_I |
| ou | | | B_WATT | | |
| | 1 | IA_FAST_RMS_I | | 20 | B_WATT_m |
| IA_FAST_RMS | 2 | IA_FAST_RMS_m | | twent | B_WATT_h |
| | | | | y one | |
| | 3 | IA_FAST_RMS_h | | twent | CFA_CNT_I |
| | | | CFA_CNT | y two | |
| | 4 | IA_RMS_I | | 23 | CFA_CNT_m |
| IA_RMS | 5 | IA_RMS_m | | 24 | CFA_CNT_h |
| | 6 | IA_RMS_h | | 25 | CFB_CNT_I |
| | 7 | IB_RMS_I | CFB_CNT | 26 | CFB_CNT_m |
| IB_RMS | 8 | IB_RMS_m | | 27 | CFB_CNT_h |
| | 9 | IB_RMS_h | | 28 | TPS1_I |
| | 10 | V_RMS_I | TPS1 | 29 | TPS1_m |
| V_RMS | 11 | V_RMS_m | | 30 | 0x00 |
| | 12 | V_RMS_h | | 31 | TPS2_I |
| | 13 | IB_FAST_RMS_I | TPS2 | 32 | TPS2_m |
| IB_FAST_RMS | 14 | IB_FAST_RMS_m | | 33 | 0x00 |
| | 15 | IB_FAST_RMS_h | checksum | 34 | checksum |
| | 16 | A_WATT_I | | | |

Full electric parameter package format:



BL0939 内置时钟免校准计量芯片

| A_WATT | 17 | A_WATT_m |
|--------|----|----------|
| | 18 | A_WATT_h |

 $\label{eq:checksum} checksum = ((\mbox{ (0x5,{A4,A3,A2,A1}) + 0x55 + data1_l + data1_m + data1_h +) \ \& \ Oxff) \ and \ invert$



3.2.7 UART Interface Protection Mechanism

The $\mathsf{UART}\xspace$ communication of $\mathsf{BL0939}\xspace$ provides a timeout protection mechanism. If the interval between bytes exceeds $\mathsf{18.5mS}\xspace$, the $\mathsf{UART}\xspace$

BL0939

The interface resets automatically.

If the frame identification byte is wrong or the CHECKSUM byte is wrong, the frame data is discarded.

 $\mathsf{UART}\xspace$ module reset: $\mathsf{RX}\xspace$ pin is pulled high after the low level exceeds $\mathsf{6.65mS}\xspace$, and the $\mathsf{UART}\xspace$ module is reset.





4 order information

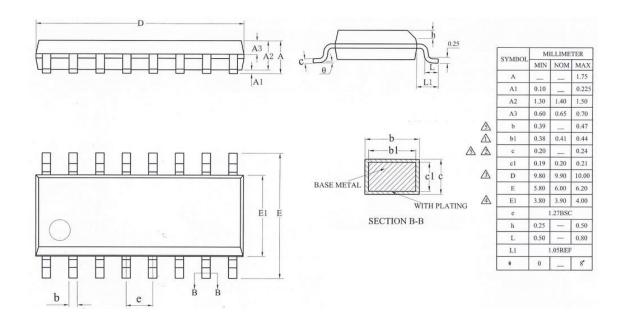
BL0939-X X=SOP16L: SOP16L encapsulation

 $\textbf{X=SSOP20L: SSOP20L} \ package$

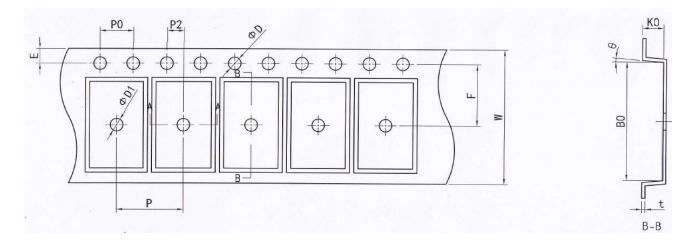
5 encapsulation

Moisture Sensitivity Level MSL 3 Warranty Period Two Years Packing method Taping packing Minimum packing 2500

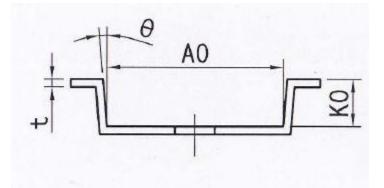
5.1 SOP16L







BL0939



A-A

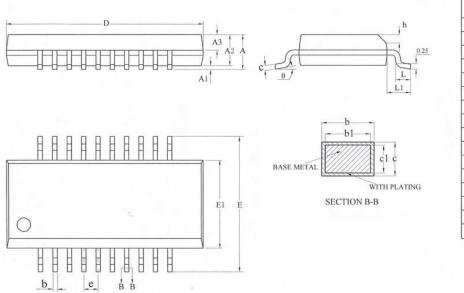
| 外观 | 尺 寸(mm) |
|------|-------------------------|
| E | 1.75±0.10 |
| F | 7.50 ± 0.05 |
| P2 | 2.00±0.10 |
| D | 1.55±0.05 |
| D1 | 1. 50 ^{+0. 25} |
| PO | 4.00±0.10 |
| 10P0 | 40.0±0.20 |

| \Box | 袋 | 5 | 寸 |
|--------|--------|-----|---|
| _ | 10.180 | - 1 | |

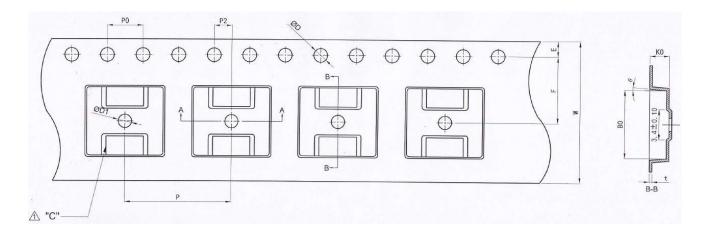
| 外观 | 尺 寸(mm) |
|----|-----------------|
| W | 16.00±0.30 |
| Р | 8.00±0.10 |
| AO | 6.70±0.10 |
| BO | 10.40±0.10 |
| KO | 2.10±0.10 |
| t | 0.30 ± 0.05 |
| θ | 5° TYP |



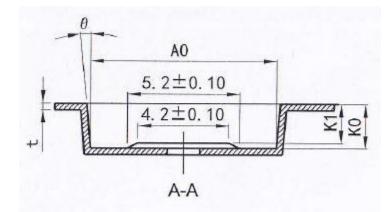
5.2 SSOP20L



| SYMBOL | М | ILLIMET | FER | |
|--------|---------|----------|------|--|
| STMBOL | MIN | NOM | MAX | |
| Α | - | - | 1.75 | |
| A1 | 0,10 | 0.15 | 0.25 | |
| A2 | 1.30 | 1.40 | 1.50 | |
| A3 | 0.60 | 0.65 | 0.70 | |
| b | 0.23 | - | 0.31 | |
| b1 | 0.22 | 0.25 | 0.28 | |
| с | 0.20 | - | 0.24 | |
| cl | 0.19 | 0.20 | 0.21 | |
| D | 8.55 | 8.65 | 8.75 | |
| Е | 5.80 | 6.00 | 6.20 | |
| EI | 3.80 | 3.90 | 4.00 | |
| e | (|).635BSC | 3 | |
| h | 0.30 | - | 0.50 | |
| L | 0.50 | - | 0.80 | |
| LI | 1.05REF | | | |
| 0 | 0 | _ | 8* | |



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共同尺寸

| 外观 | 尺 寸(mm) |
|------|------------------------|
| E | 1.75±0.10 |
| F | 7.50±0.10 |
| P2 | 2.00±0.10 |
| D | 1.55±0.05 |
| D1 | 1. 5 ^{+0. 25} |
| PO | 4 .00±0.10 |
| 10P0 | 40.00±0.20 |

口袋尺寸 外观 尺 寸(mm) 2 16.00±0.20 W 12.00±0.10 P 3 8.40±0.10 AO \$ \$ 7.75±0.10 BO 2.50 ± 0.10 K0 t 0.30 ± 0.05 3~5° TYP θ 3 K1 2.10 ± 0.10

BL0939