74LVC125A

Quad buffer/line driver with 5 V tolerant input/outputs; 3-state

Rev. 12 — 2 May 2025 Product data sheet

1. General description

The 74LVC125A is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs ($n\overline{OE}$). A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC125AD	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC125APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC125ABQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74LVC125ABZ	-40 °C to +125 °C	DHXQFN14	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm × 2 mm × 0.48 mm	SOT8014-1

4. Functional diagram

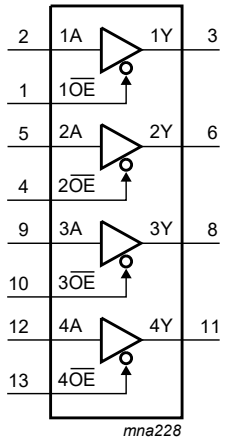


Fig. 1. Logic symbol

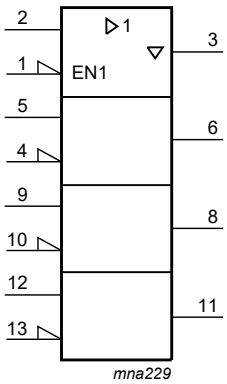


Fig. 2. IEC logic symbol

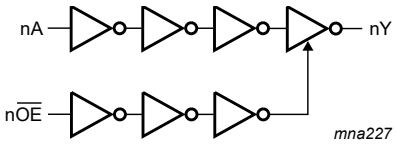
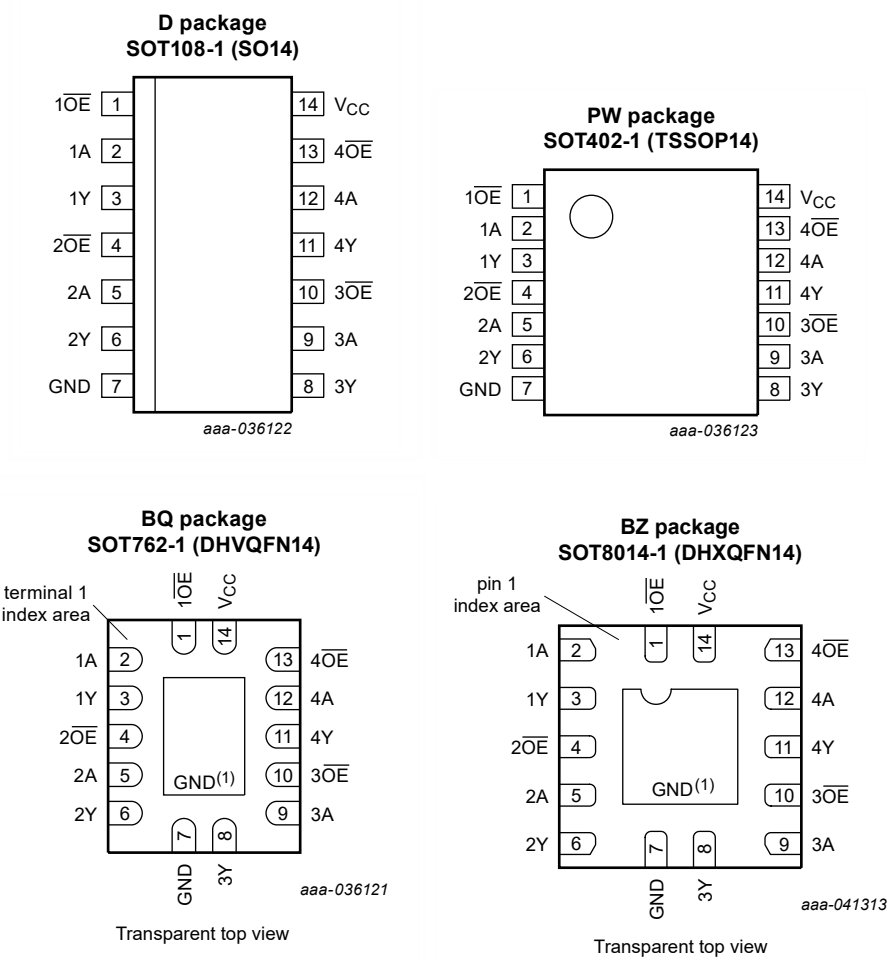


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	1, 4, 10, 13	data enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Inputs		Output
n$\overline{OE}$	**nA**	**nY**
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW-state	[2]	-0.5	V_{CC} + 0.5	V
		output 3-state	[2]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C				
		SOT108-1 (SO14) SOT402-1 (TSSOP14) SOT762-1 (DHVQFN14)	[3]	-	500	mW
		SOT8014-1 (DHXQFN14)	[4]	-	250	mW
T_{stg}	storage temperature			-65	+150	°C

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.
[4] For SOT8014-1 (DHXQFN14) package: P_{tot} derates linearly with 8.7 mW/K above 121 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.3 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V_{CC} = 1.65 V to 1.95 V	$0.65V_{CC}$	-	-	$0.65V_{CC}$	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V_{CC} = 1.65 V to 1.95 V	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.65 V to 3.6 V	V_{CC} - 0.2	-	-	V_{CC} - 0.3	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I_O = -18 mA; V_{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.8	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I_I	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 3.6 V; V_O = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I_{OFF}	power-off leakage current	V_{CC} = 0.0 V; V_I or V_O = 5.5 V	-	±0.1	±10	-	±20	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V	-	5	500	-	5000	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND to V_{CC}	-	4.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

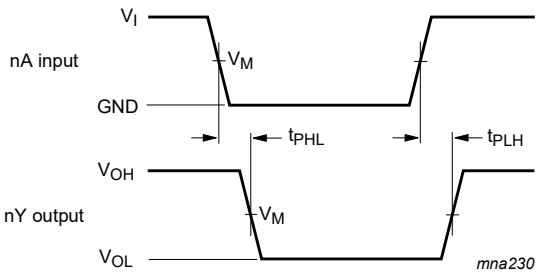
Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 4 [2]						
		V_{CC} = 1.2 V	-	12.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.5	5.4	11.0	1.5	12.8	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.9	5.7	1.0	6.7	ns
		V_{CC} = 2.7 V	1.5	2.8	5.5	1.5	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.5	4.8	1.0	6.0	ns
t_{en}	enable time	$n\overline{OE}$ to nY; see Fig. 5 [2]						
		V_{CC} = 1.2 V	-	16.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.0	5.0	12.2	1.0	14.2	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.9	6.8	0.5	7.9	ns
		V_{CC} = 2.7 V	1.5	3.1	6.6	1.5	8.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	5.4	1.0	7.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nY; see Fig. 5 [2]						
		V_{CC} = 1.2 V	-	7.0	-	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	2.2	4.6	7.5	2.2	8.7	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.6	4.2	0.5	5.0	ns
		V_{CC} = 2.7 V	1.5	3.1	5.0	1.5	6.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	4.6	1.0	6.0	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{sk(o)}$	output skew time	V_{CC} = 3.0 V to 3.6 V [3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [4]						
		V_{CC} = 1.65 V to 1.95 V	-	6.0	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	9.4	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	12.4	-	-	-	pF

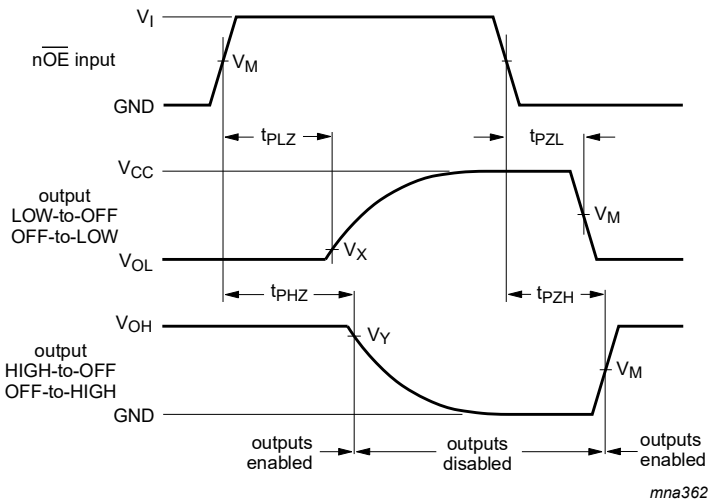
[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The input nA to output nY propagation delays

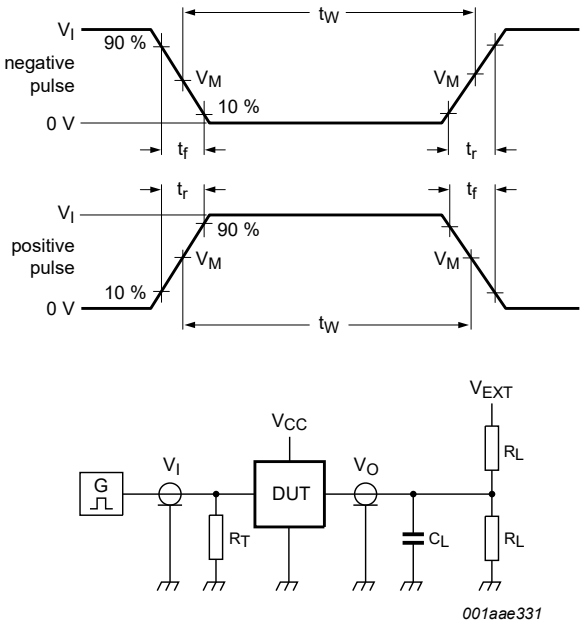


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
1.65 V to 1.95 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

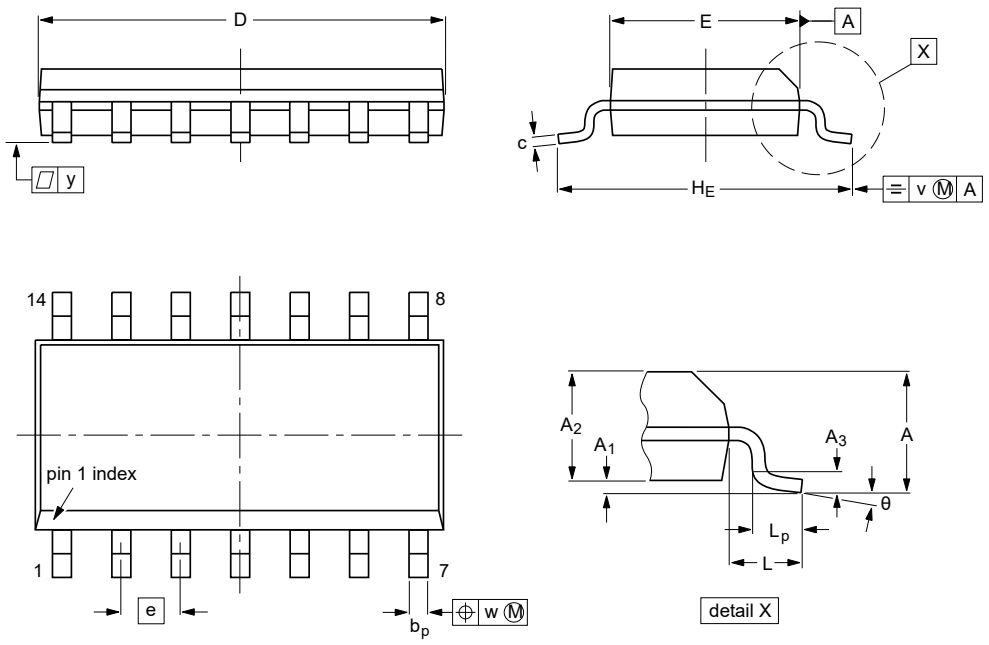
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

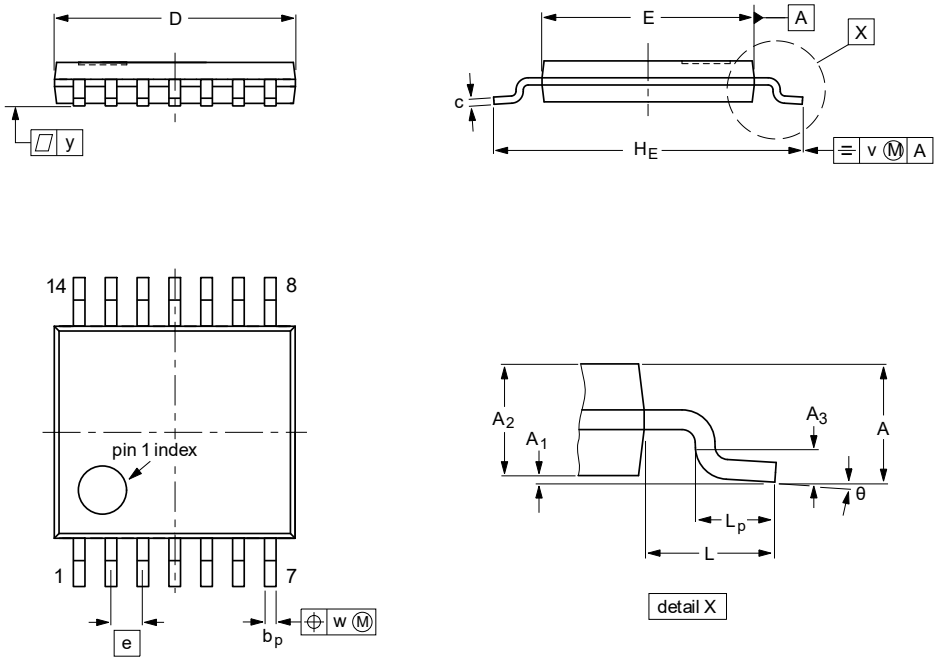
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

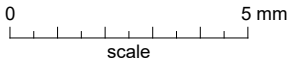
sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

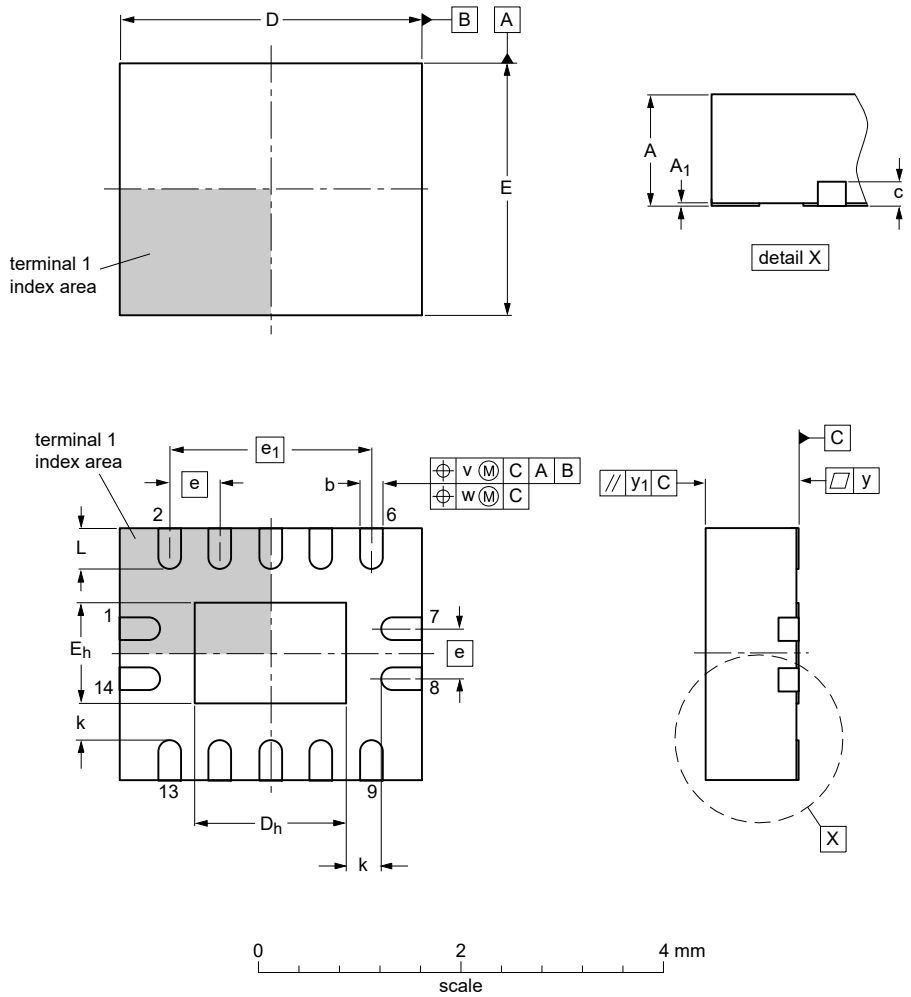
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

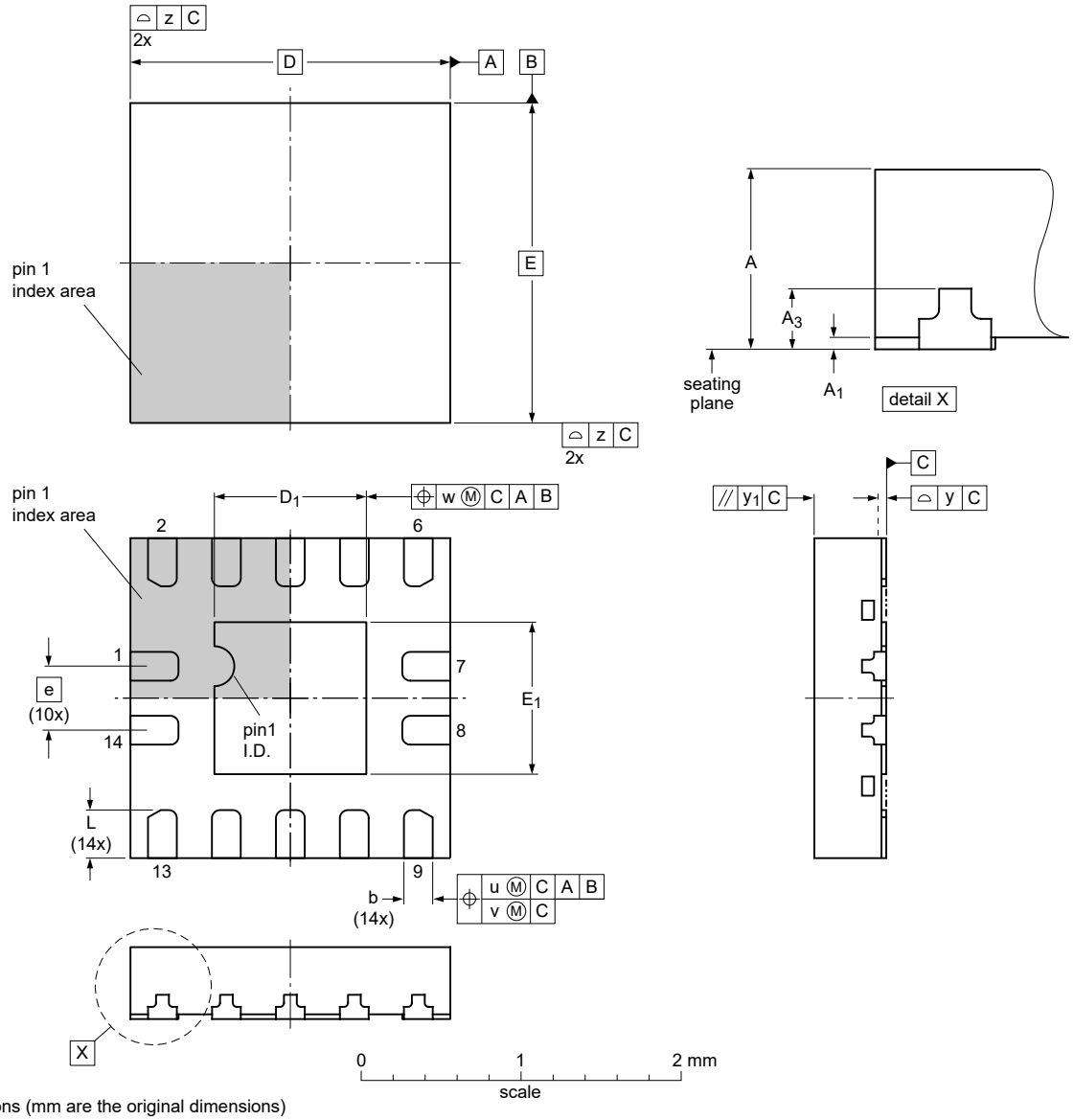
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 9. Package outline SOT762-1 (DHVQFN14)

DHXQFN14: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm x 2 mm x 0.48 mm **SOT8014-1**



Dimensions (mm are the original dimensions)

Unit	A	A_1	A_3	b	D	D_1	E	E_1	e	k	L	u	v	w	y	y_1	z
max	0.48	0.05	0.15 (typ)	0.23	2.0	1.00	2.0	1.00	0.4	0.2	0.35	0.1	0.05	0.1	0.05	0.05	0.05
mm nom	0.45	0.02		0.18		0.95		0.95			0.30						
min	0.42	0.00		0.13		0.90		0.90			0.25						

sot8014-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8014-1						~~20-09-18~~ 20-09-22

Fig. 10. Package outline SOT8014-1 (DHXQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC125A v.12	20250502	Product data sheet	-	74LVC125A v.11
Modifications:	• Type number 74LVC125ABZ (SOT8014-1/DHXQFN14) added.			
74LVC125A v.11	20240212	Product data sheet	-	74LVC125A v.10
Modifications:	• Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LVC125A v.10	20230803	Product data sheet	-	74LVC125A v.9
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC125A v.9	20210917	Product data sheet	-	74LVC125A v.8
Modifications:	• Type number 74LVC125ADB (SOT337-1/SSOP14) removed. • Section 1 and Section 2 updated.			
74LVC125A v.8	20200505	Product data sheet	-	74LVC125A v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 4: Derating values for P_{tot} total power dissipation updated. • Table 8: Added measurement points for V_X and V_Y. • Fig. 9: Package outline drawing SOT762-1 (DHVQFN14) updated.			
74LVC125A v.7	20130411	Product data sheet	-	74LVC125A v.6
Modifications:	• Features list corrected (errata)			
74LVC125A v.6	20130305	Product data sheet	-	74LVC125A v.5
74LVC125A v.5	20120208	Product data sheet	-	74LVC125A v.4
74LVC125A v.4	20030507	Product specification	-	74LVC125A v.3
74LVC125A v.3	20020308	Product specification	-	74LVC125A v.2
74LVC125A v.2	19980428	Product specification	-	74LVC125A v.1
74LVC125A v.1	19970801	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 2 May 2025