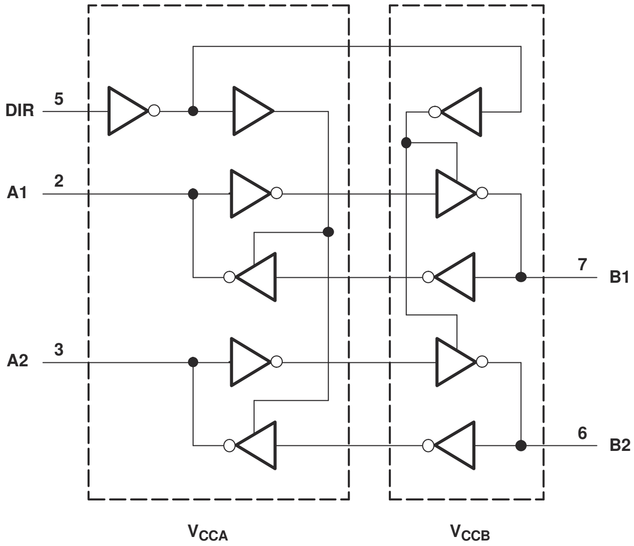
SN74LVC2T45 Dual-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation

1 Features

- Fully configurable dual-rail design allows each port to operate over the full 1.65-V to 5.5-V power-supply range
- V_{CC} isolation feature – if either V_{CC} input is at GND, both ports are in the high-impedance state
- DIR input circuit referenced to V_{CCA}
- Low power consumption, 4-µA maximum I_{CC}
- Available in the Texas Instruments NanoFree™ package
- ±24-mA output drive at 3.3 V
- I_{off} supports Partial-Power-Down mode operation
- Maximum data rates:
  - 420 Mbps (3.3-V to 5-V translation)
  - 210 Mbps (translate to 3.3 V)
  - 140 Mbps (translate to 2.5 V)
  - 75 Mbps (translate to 1.8 V)
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 4000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Personal electronic
- Industrial
- Enterprise
- Telecom



Functional Block Diagram

3 Description

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65V to 5.5V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 5.5V. This allows for universal low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

The SN74LVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports are always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74LVC2T45 is designed so that V_{CCA} supplies the DIR input circuit. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature is designed so that if either V_{CC} input is at GND, both ports are in the high-impedance state.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74LVC2T45	DCT (SM8, 8)	2.95mm × 4mm
	DCU (VSSOP, 8)	2mm × 3.1mm
	YZP (DSBGA, 8)	1.5mm × 0.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Pin Configuration and Functions

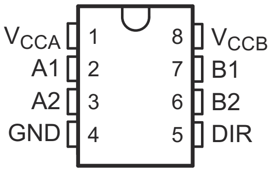

Figure 4-1. DCT or DCU Package, 8-Pin SM8 or VSSOP (Top View)

Table 4-1. Pin Functions: DCT, DCU

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
V_{CCA}	1	P	A-port supply voltage. 1.65V ≤ V_{CCA} ≤ 5.5V
A1	2	I/O	Input/output A1. Referenced to V_{CCA}
A2	3	I/O	Input/output A2. Referenced to V_{CCA}
GND	4	G	Ground
DIR	5	I	Direction control signal
B2	6	I/O	Input/output B2. Referenced to V_{CCB}
B1	7	I/O	Input/output B1. Referenced to V_{CCB}
V_{CCB}	8	P	B-port supply voltage. 1.65V ≤ V_{CCB} ≤ 5.5V

(1) I = input, O = output, P = power, G =ground

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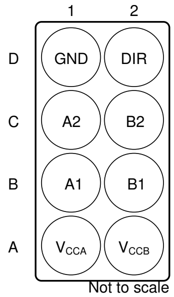

Figure 4-2. YZP Package, 8-Pin DSGBA (Bottom View)

Table 4-2. Pin Functions: YZP

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
A1	V_{CCA}	P	A-port supply voltage. 1.65V ≤ V_{CCA} ≤ 5.5V
A2	V_{CCB}	P	B-port supply voltage. 1.65V ≤ V_{CCB} ≤ 5.5V
B1	A1	I/O	Input/output A1. Referenced to V_{CCA}
B2	B1	I/O	Input/output B1. Referenced to V_{CCB}
C1	A2	I/O	Input/output A2. Referenced to V_{CCA}
C2	B2	I/O	Input/output B2. Referenced to V_{CCB}
D1	GND	G	Ground
D2	DIR	I	Direction control signal

(1) I = input, O = output, P = power, G = ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	6.5	V
V_{CCB}					
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 [2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.65	5.5	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs(4)	1.65V to 1.95V		V_{CCI} × 0.65		V
			2.3V to 2.7V		1.7		
			3V to 3.6V		2		
			4.5V to 5.5V		V_{CCI} × 0.7		
V_{IL}	Low-level input voltage	Data inputs(4)	1.65V to 1.95V			V_{CCI} × 0.35	V
			2.3V to 2.7V			0.7	
			3V to 3.6V			0.8	
			4.5V to 5.5V			V_{CCI} × 0.3	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	1.65V to 1.95V		V_{CCA} × 0.65		V
			2.3V to 2.7V		1.7		
			3V to 3.6V		2		
			4.5V to 5.5V		V_{CCA} × 0.7		

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5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	1.65V to 1.95V			V_{CCA} × 0.35	V
			2.3V to 2.7V			0.7	
			3V to 3.6V			0.8	
			4.5V to 5.5V			V_{CCA} × 0.3	
V_I	Input voltage				0	5.5	V
V_O	Output voltage				0	V_{CCO}	V
I_{OH}	High-level output current			1.65V to 1.95V		–4	mA
				2.3V to 2.7V		–8	
				3V to 3.6V		–24	
				4.5V to 5.5V		–32	
I_{OL}	Low-level output current			1.65V to 1.95V		4	mA
				2.3V to 2.7V		8	
				3V to 3.6V		24	
				4.5V to 5.5V		32	
Δt/Δv	Input transition rise or fall rate	Data inputs	1.65V to 1.95V			20	ns/V
			2.3V to 2.7V			20	
			3V to 3.6V			10	
			4.5V to 5.5V			5	
		Control input	1.65V to 5.5V			5	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND for proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V.

5.4 Thermal Information

THERMAL METRIC(1)		SN74LVC2T45			UNIT
		DCU	DCT	YZP	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	246.4	195.3	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.4	106	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	157.8	110.8	10.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	37	38.3	3.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	156.9	109.3	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1] [2]

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to +85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100μA	V_I = V_{IH}	1.65V to 4.5V	1.65V to 4.5V				V_{CCO} – 0.1		V
		I_{OH} = –4mA		1.65V	1.65V				1.2		
		I_{OH} = –8mA		2.3V	2.3V				1.9		
		I_{OH} = –24mA		3V	3V				2.4		
		I_{OH} = –32mA		4.5V	4.5V				3.8		
V_{OL}		I_{OL} = 100μA	V_I = V_{IL}	1.65V to 4.5V	1.65V to 4.5V					0.1	V
		I_{OL} = 4mA		1.65V	1.65V					0.45	
		I_{OL} = 8mA		2.3V	2.3V					0.3	
		I_{OL} = 24mA		3V	3V					0.55	
		I_{OL} = 32mA		4.5V	4.5V					0.55	
I_I	DIR	V_I = V_{CCA} or GND		1.65V to 5.5V	1.65V to 5.5V			±1		±2	μA
I_{off}	A port	V_I or V_O = 0 to 5.5V		0V	0 to 5.5V			±1		±2	μA
	B port			0 to 5.5V	0V			±1		±2	
I_{OZ}	A or B port	V_O = V_{CCO} or GND		1.65V to 5.5V	1.65V to 5.5V			±1		±2	μA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0		1.65V to 5.5V	1.65V to 5.5V					3	μA
				5V	0V					2	
				0V	5V					–2	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0		1.65V to 5.5V	1.65V to 5.5V					3	μA
				5V	0V					–2	
				0V	5V					2	
I_{CCA} + I_{CCB} (see Table 8-4)		V_I = V_{CCI} or GND, I_O = 0		1.65V to 5.5V	1.65V to 5.5V					4	μA
ΔI_{CCA}	A port	One A port at V_{CCA} – 0.6V, DIR at V_{CCA}, B port = open		3V to 5.5V	3V to 5.5V					50	μA
	DIR	DIR at V_{CCA} – 0.6V, B port = open, A port at V_{CCA} or GND								50	
ΔI_{CCB}	B port	One B port at V_{CCB} – 0.6V, DIR at GND, A port = open		3V to 5.5V	3V to 5.5V					50	μA
C_I	DIR	V_I = V_{CCA} or GND		3.3V	3.3V		2.5				pF
C_{io}	A or B port	V_O = $V_{CCA/B}$ or GND		3.3V	3.3V		6				pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

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5.6 Switching Characteristics: V_{CCA} = 1.8V ± 0.15V

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	17.7	2.2	10.3	1.7	8.3	1.4	7.2	ns
t_{PHL}			2.8	14.3	2.2	8.5	1.8	7.1	1.7	7	
t_{PLH}	B	A	3	17.7	2.3	16	2.1	15.5	1.9	15.1	ns
t_{PHL}			2.8	14.3	2.1	12.9	2	12.6	1.8	12.2	
t_{PHZ}	DIR	A	5.5	30.9	5.5	30.5	5.5	30.5	5.5	29.3	ns
t_{PLZ}			4.3	19.7	4.2	19.6	4.1	19.5	4	19.4	
t_{PHZ}	DIR	B	6	27.9	5	14.9	5	11.3	4.1	8.6	ns
t_{PLZ}			5	19.5	3.9	12.6	4.3	9.7	2.1	7.1	
t_{PZH} [1]	DIR	A		37.2		28.6		25.2		22.2	ns
t_{PZL} [1]				42.2		27.8		23.9		20.8	
t_{PZH} [1]	DIR	B		37.4		29.9		27.8		26.6	ns
t_{PZL} [1]				45.2		39		37.6		36.3	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

5.7 Switching Characteristics: V_{CCA} = 2.5V ± 0.2V

over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	16	1.5	8.5	1.3	6.4	1.1	5.1	ns
t_{PHL}			2.1	12.9	1.4	7.5	1.3	5.4	0.9	4.6	
t_{PLH}	B	A	2.2	10.3	1.5	8.5	1.4	8	1	7.5	ns
t_{PHL}			2.2	8.5	1.4	7.5	1.3	7	0.9	6.2	
t_{PHZ}	DIR	A	4.2	17.1	4.2	16.8	4.1	16.8	4.1	16.5	ns
t_{PLZ}			3.2	12.6	3.2	12.5	3.2	12.3	3	12.3	
t_{PHZ}	DIR	B	6	27.9	4.7	13.9	4.7	10.5	3.5	7.6	ns
t_{PLZ}			4.2	18.9	3.6	11.2	3.6	8.9	1.4	6.2	
t_{PZH} [1]	DIR	A		29.2		19.7		16.9		13.7	ns
t_{PZL} [1]				36.4		21.4		17.5		13.8	
t_{PZH} [1]	DIR	B		28.6		21		18.7		17.4	ns
t_{PZL} [1]				30		24.3		22.2		21.1	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

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5.8 Switching Characteristics: V_{CCA} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	15.5	1.4	8	0.7	5.6	0.7	4.4	ns
t_{PHL}			2	12.6	1.3	7	0.8	5	0.7	4	
t_{PLH}	B	A	1.7	8.3	1.3	6.4	0.7	5.8	0.6	5.4	ns
t_{PHL}			1.8	7.1	1.3	5.4	0.8	5	0.7	4.5	
t_{PHZ}	DIR	A	4.5	10.9	4.5	10.8	4.4	10.8	4.4	10.4	ns
t_{PLZ}			3.4	8.4	3.7	8.4	3.9	8.1	3.3	7.8	
t_{PHZ}	DIR	B	5.7	27.3	4.7	13.7	4.7	10.4	2.9	7.4	ns
t_{PLZ}			4.5	17.7	3.5	11.3	4.3	8.3	1	5.6	
t_{PZH} [1]	DIR	A		26		17.7		14.1		11	ns
t_{PZL} [1]				34.4		19.1		15.4		11.9	
t_{PZH} [1]	DIR	B		23.9		16.4		13.9		12.2	ns
t_{PZL} [1]				23.5		17.8		15.8		14.4	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

5.9 Switching Characteristics: V_{CCA} = 5V ± 0.5V

over recommended operating free-air temperature range, V_{CCA} = 5V ± 0.5V (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8V ±0.15V		V_{CCB} = 2.5V ±0.2V		V_{CCB} = 3.3V ±0.3V		V_{CCB} = 5V ±0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	15.1	1	7.5	0.6	5.4	0.5	3.9	ns
t_{PHL}			1.8	12.2	0.9	6.2	0.7	4.5	0.5	3.5	
t_{PLH}	B	A	1.4	7.2	1	5.1	0.7	4.4	0.5	3.9	ns
t_{PHL}			1.7	7	0.9	4.6	0.7	4	0.5	3.5	
t_{PHZ}	DIR	A	2.9	8.2	2.9	7.9	2.8	7.9	2.2	7.8	ns
t_{PLZ}			1.4	6.9	1.3	6.7	0.7	6.7	0.7	6.6	
t_{PHZ}	DIR	B	5.8	26.1	4.4	13.9	4.4	10.1	1.3	7.3	ns
t_{PLZ}			4.7	16.9	3.3	11	4	7.7	1	5.6	
t_{PZH} [1]	DIR	A		24.1		16.1		12.1		9.5	ns
t_{PZL} [1]				33.1		18.5		14.1		10.8	
t_{PZH} [1]	DIR	B		22		14.2		12.1		10.5	ns
t_{PZL} [1]				20.4		14.1		12.4		11.3	

(1) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

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5.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.8V	V_{CCA} = V_{CCB} = 2.5V	V_{CCA} = V_{CCB} = 3.3V	V_{CCA} = V_{CCB} = 5V	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0pF, f = 10MHz, t_r = t_f = 1ns	3	4	4	4	pF
	B-port input, A-port output		18	19	20	21	
C_{pdB} (1)	A-port input, B-port output	C_L = 0pF, f = 10MHz, t_r = t_f = 1ns	18	19	20	21	pF
	B-port input, A-port output		3	4	4	4	

(1) Power dissipation capacitance per transceiver.

5.11 Typical Characteristics

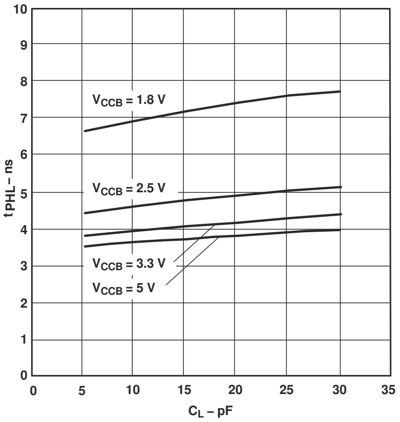

Figure 5-1. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.8V

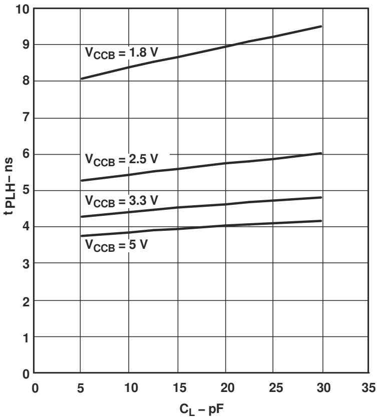

Figure 5-2. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.8V

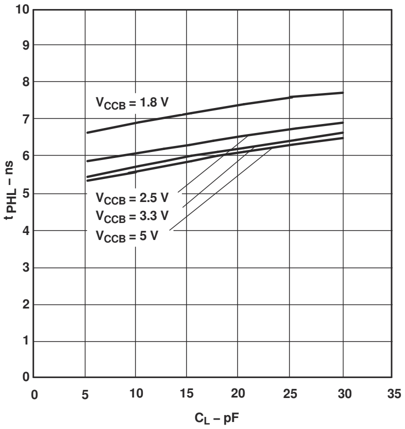

Figure 5-3. Typical Propagation Delay of High-to-Low (B to A) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.8V

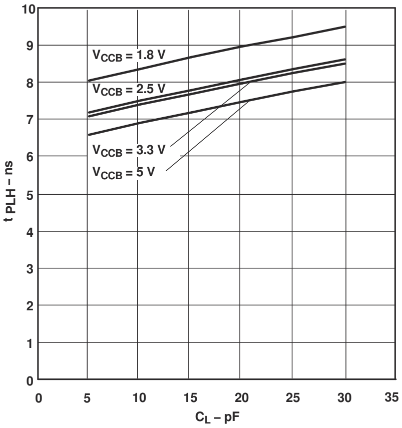

Figure 5-4. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance T_A = 25°C, V_{CCA} = 1.8V

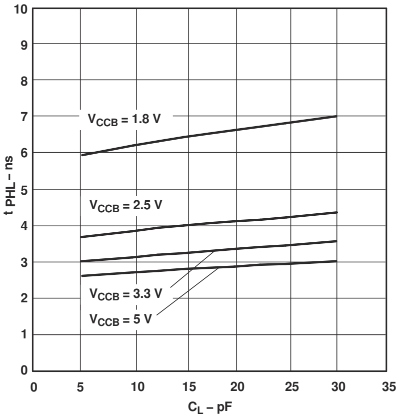

Figure 5-5. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 2.5V

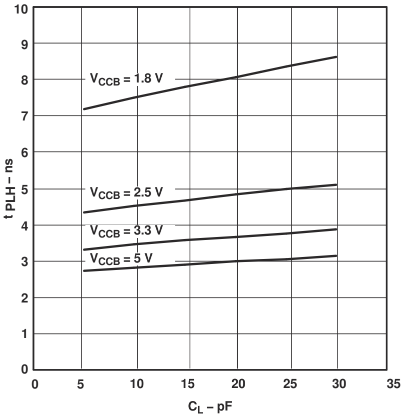

Figure 5-6. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 2.5V

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5.11 Typical Characteristics (continued)

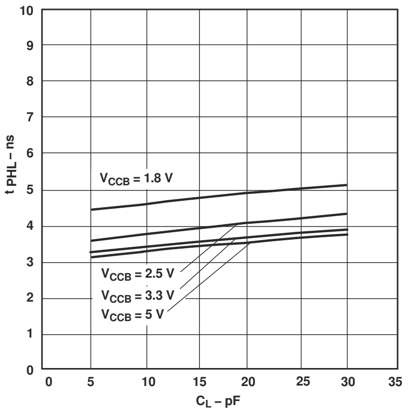

Figure 5-7. Typical Propagation Delay of High-to-Low (B to A) vs Load Capacitance T_A = 25°C, V_{CCA} = 2.5V

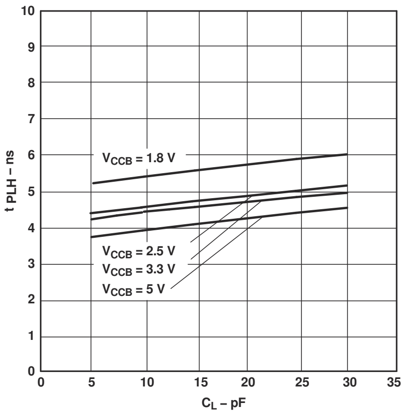

Figure 5-8. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance T_A = 25°C, V_{CCA} = 2.5V

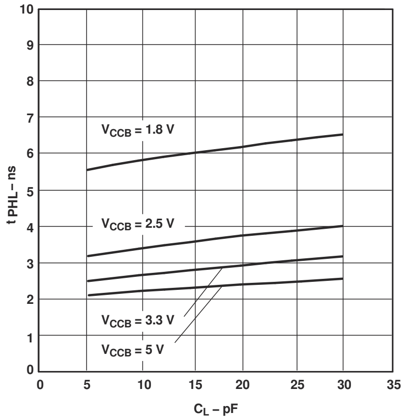

Figure 5-9. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 3.3V

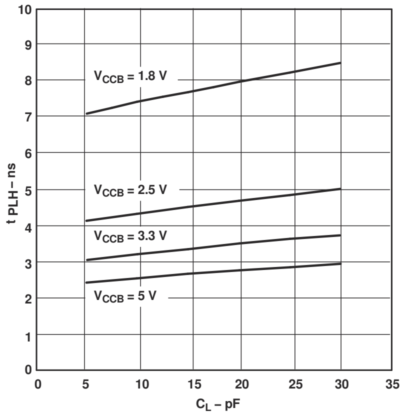

Figure 5-10. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 3.3V

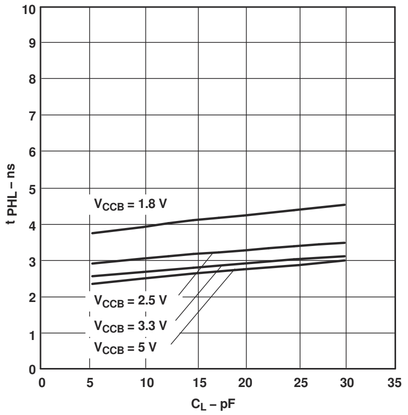

Figure 5-11. Typical Propagation Delay of High-to-Low (B to A) vs Load Capacitance T_A = 25°C, V_{CCA} = 3.3V

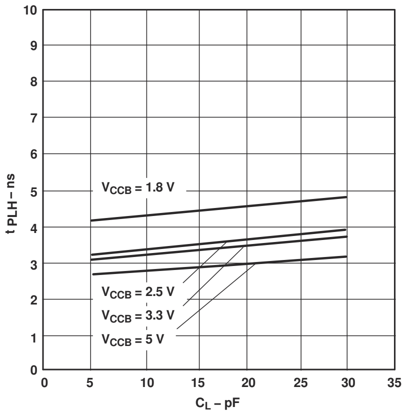

Figure 5-12. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance T_A = 25°C, V_{CCA} = 3.3V

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5.11 Typical Characteristics (continued)

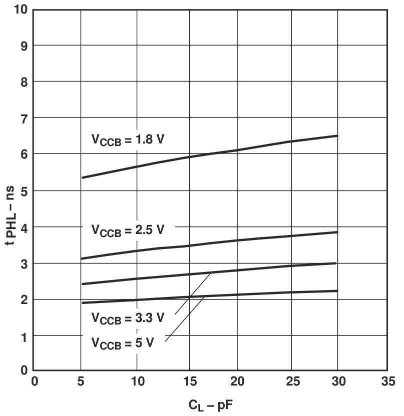

Figure 5-13. Typical Propagation Delay of High-to-Low (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 5V

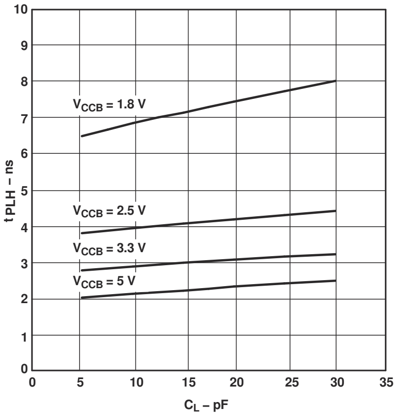

Figure 5-14. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance T_A = 25°C, V_{CCA} = 5V

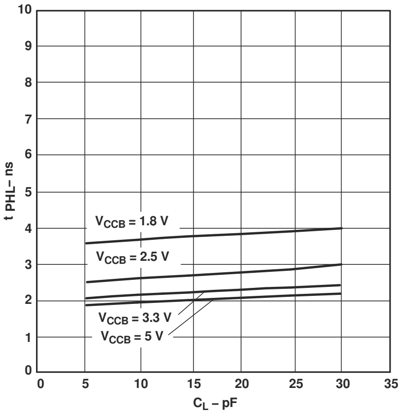

Figure 5-15. Typical Propagation Delay of High-to-Low (B to A) vs Load Capacitance T_A = 25°C, V_{CCA} = 5V

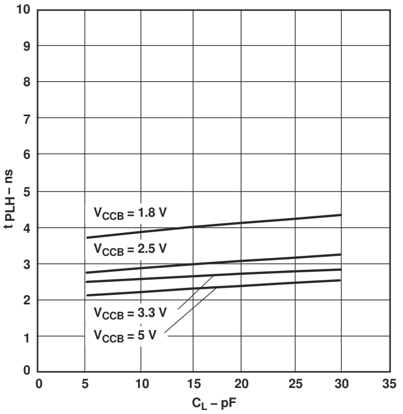

Figure 5-16. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance T_A = 25°C, V_{CCA} = 5V

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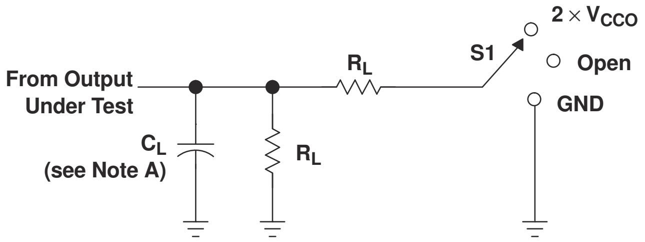
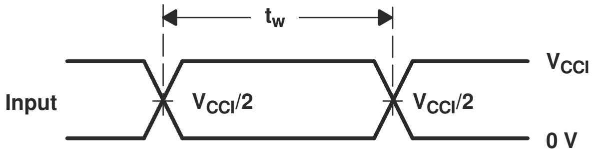
6 Parameter Measurement Information



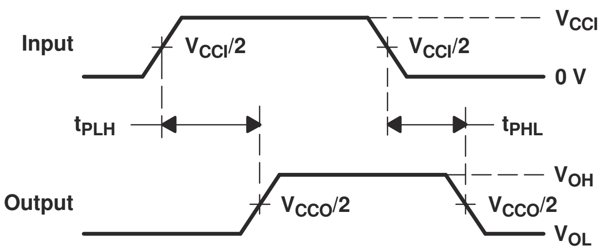
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

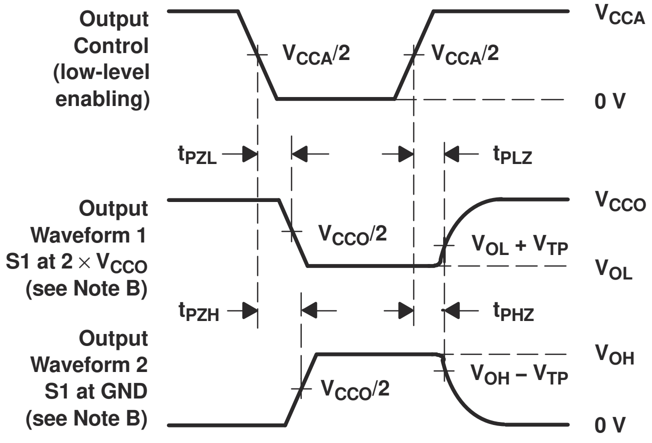


VOLTAGE WAVEFORMS
PULSE DURATION

V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V
5 V ± 0.5 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74LVC2T45 is a dual-bit, dual-supply noninverting voltage level translation device. V_{CCA} supports pin Ax and the direction control pin, and V_{CCB} supports pin Bx. The A port can accept I/O voltages ranging from 1.65V to 5.5V, while the B port can accept I/O voltages from 1.65V to 5.5V. The high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A.

7.2 Functional Block Diagram

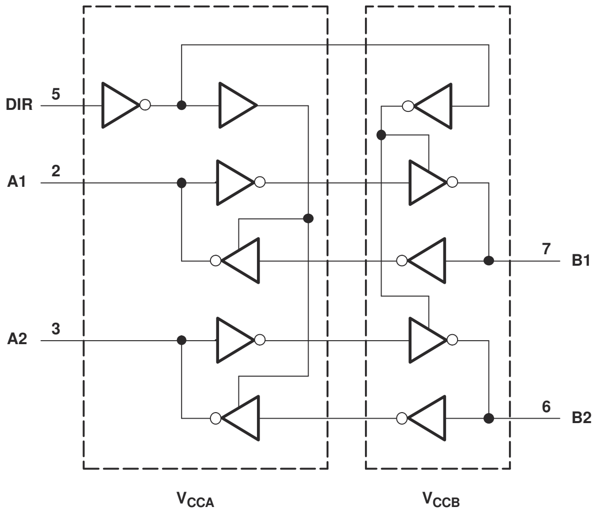

Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65V to 5.5V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.65V and 5.5V making the device suitable for translating between any of the voltage nodes (1.8V, 2.5V, 3.3V, and 5V).

7.3.2 Support High-Speed Translation

SN74LVC2T45 can support high data rate applications. The translated signal data rate can be up to 420Mbps when signal is translated from 3.3V to 5V.

7.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when the device is in Partial-Power-Down mode. The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.3.4 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so impedance matching and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Two outputs can be connected together for a stronger output drive strength. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

7.3.5 Glitch-Free Power Supply Sequencing

Either supply rail may be powered on or off in any order without producing a glitch on the I/Os (that is, where the output erroneously transitions to VCC when it should be held low or vice versa). Glitches of this nature can

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be misinterpreted by a peripheral as a valid data bit, which could trigger a false device reset of the peripheral, a false device configuration of the peripheral, or even a false data initialization by the peripheral.

7.3.6 V_{CC} Isolation

The I/Os of both ports will enter a high-impedance state when either of the supplies are at GND, while the other supply is still connected to the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVC2T45 device.

Table 7-1. Function Table (Each Transceiver)(1)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC2T45 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum data rate can be up to 420Mbps when the device translates signal from 3.3V to 5V. It is recommended to tie all unused I/Os to GND. The device should not have any floating I/Os when changing translation direction.

8.2 Typical Applications

8.2.1 Unidirectional Logic Level-Shifting Application

Figure 8-1 shows an example of the SN74LVC2T45 being used in a unidirectional logic level-shifting application.

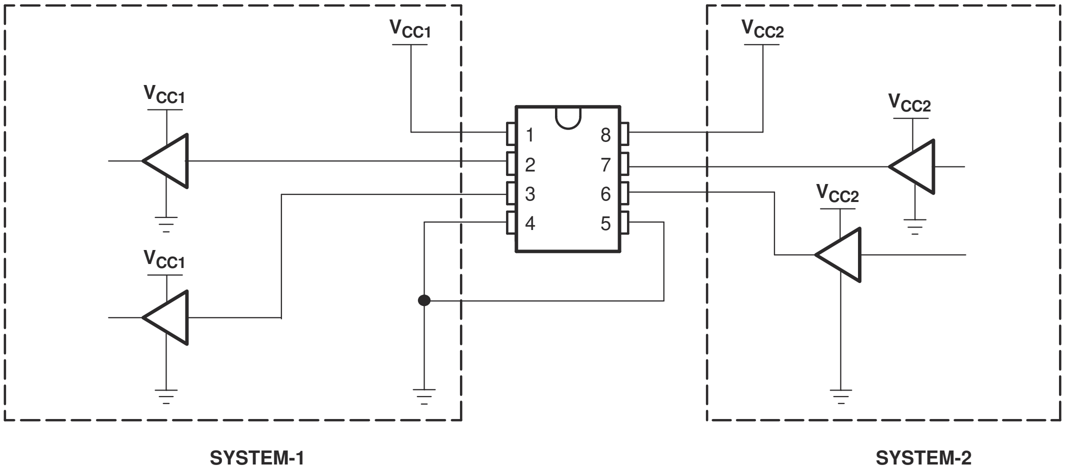


Figure 8-1. Unidirectional Logic Level-Shifting Application

8.2.1.1 Design Requirements

Table 8-1 lists the pins and pin descriptions of the SN74LVC2T45 connections with SYSTEM-1 and SYSTEM-2.

Table 8-1. SN74LVC2T45 Pin Connections With SYSTEM-1 and SYSTEM-2

PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (1.65V to 5.5V)
2	A1	OUT1	Output level depends on V_{CC1} voltage.
3	A2	OUT2	Output level depends on V_{CC1} voltage.
4	GND	GND	Device GND
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	B2	IN2	Input threshold value depends on V_{CC2} voltage.
7	B1	IN1	Input threshold value depends on V_{CC2} voltage.
8	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (1.65V to 5.5V)

For this design example, use the parameters listed in Table 8-2.

Table 8-2. Design Parameters

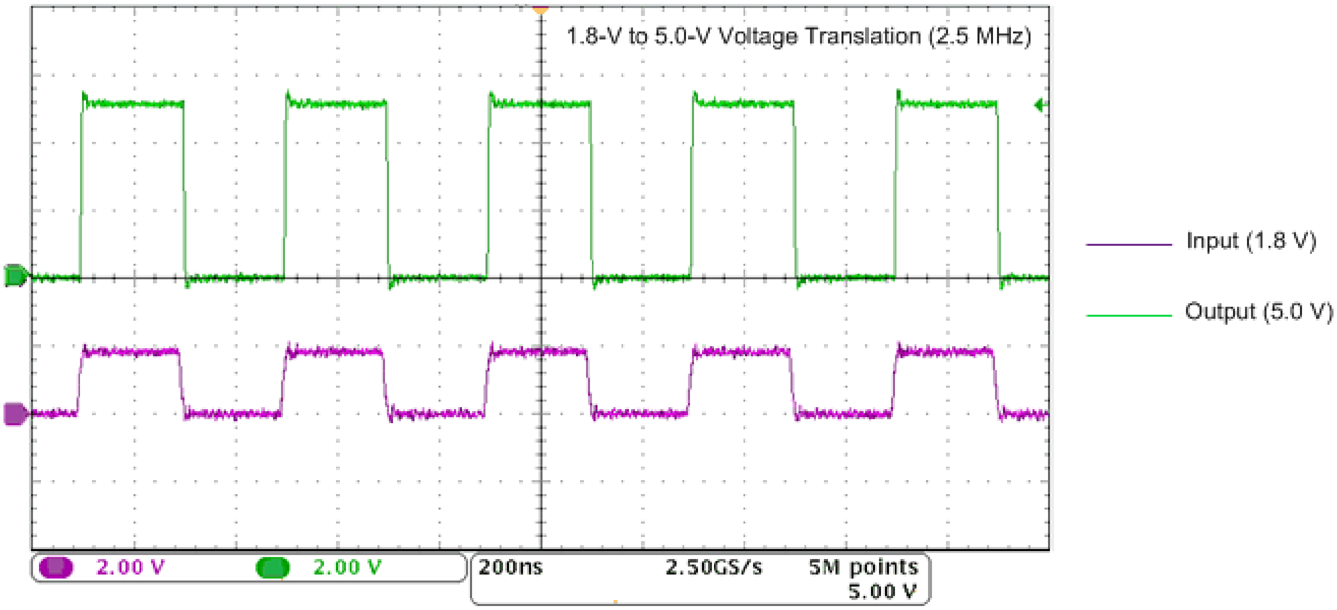
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65V to 5.5V
Output voltage range	1.65V to 5.5V

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74LVC2T45 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74LVC2T45 device is driving to determine the output voltage range.

8.2.1.3 Application Curve



8.2.2 Bidirectional Logic Level-Shifting Application

Figure 8-2 shows the SN74LVC2T45 being used in a bidirectional logic level-shifting application. Because the SN74LVC2T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

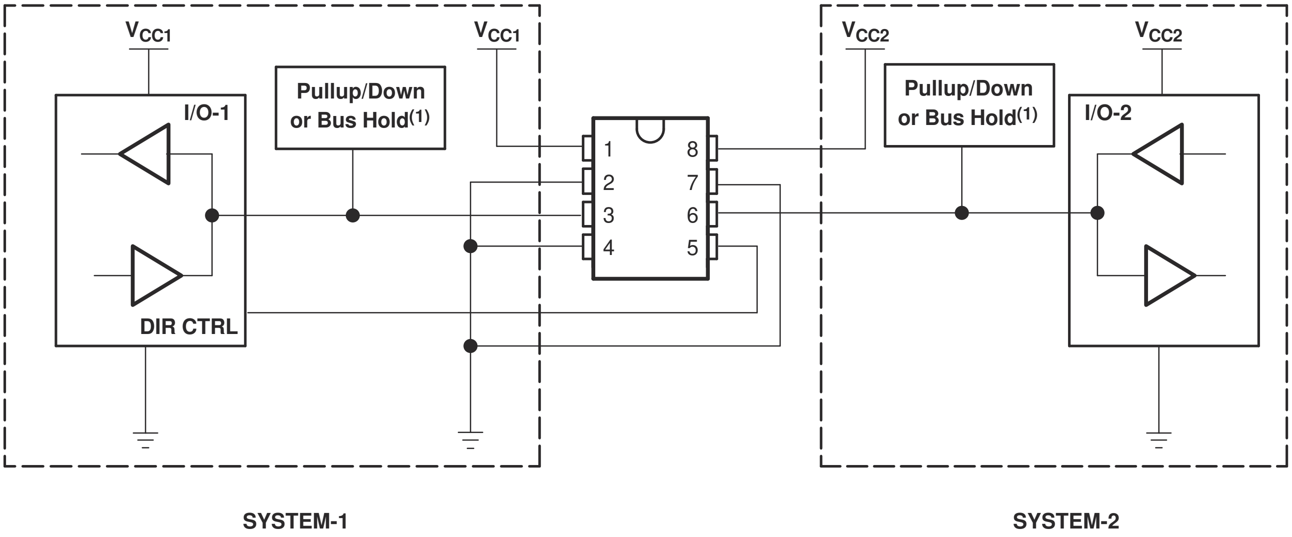


Figure 8-2. Bidirectional Logic Level-Shifting Application

8.2.2.1 Design Requirements

Refer to *Section 8.2.1*.

8.2.2.2 Detailed Design Procedure

Table 8-3 provides data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

Table 8-3. Data Transmission Sequence

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

8.2.2.2.1 Enable Times

Calculate the enable times for the SN74LVC2T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

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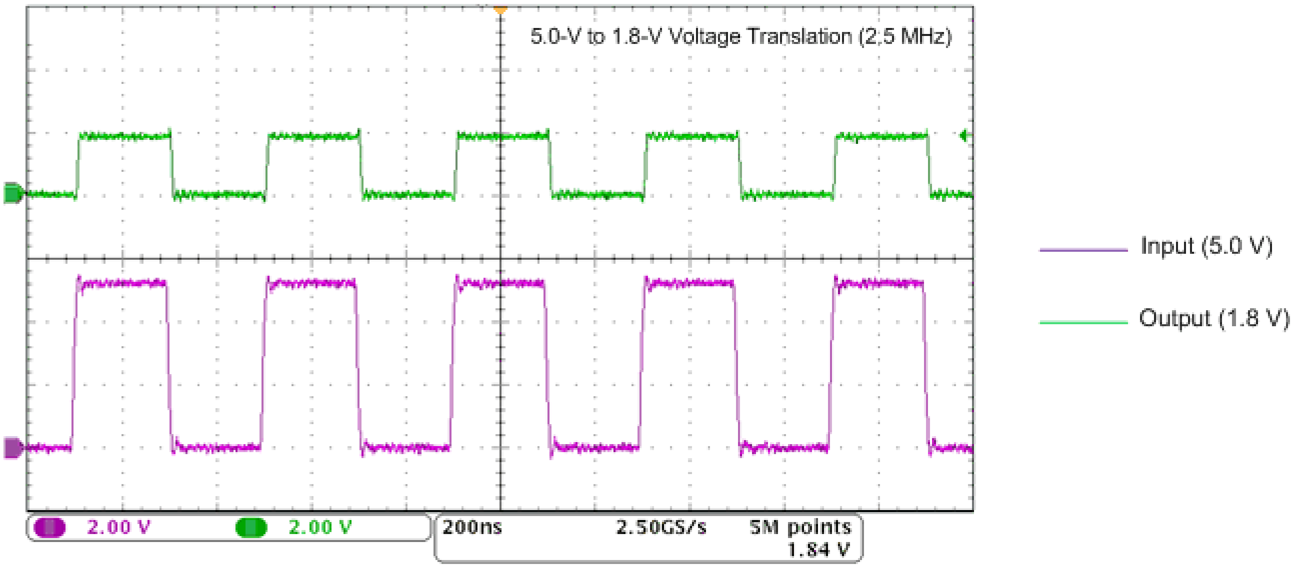
8.2.2.3 Application Curve



8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices, as described in *Glitch-free Power Supply Sequencing*.

8.3.1 Power-Up Consideration

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1μF is recommended. If there are multiple V_{CC} pins, 0.01μF or 0.022μF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

Table 8-4. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}					UNIT
	0V	**1.8V**	**2.5V**	**3.3V**	**5V**	
0V	0	< 1	< 1	< 1	< 1	μA
1.8V	< 1	< 2	< 2	< 2	2	
2.5V	< 1	< 2	< 2	< 2	< 2	
3.3V	< 1	< 2	< 2	< 2	< 2	
5V	< 1	2	< 2	< 2	< 2	

8.4 Layout

8.4.1 Layout Guidelines

It is recommended to follow common printed-circuit board layout guidelines for device reliability, such as the follows:

- Use bypass capacitors on the power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

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8.4.2 Layout Example

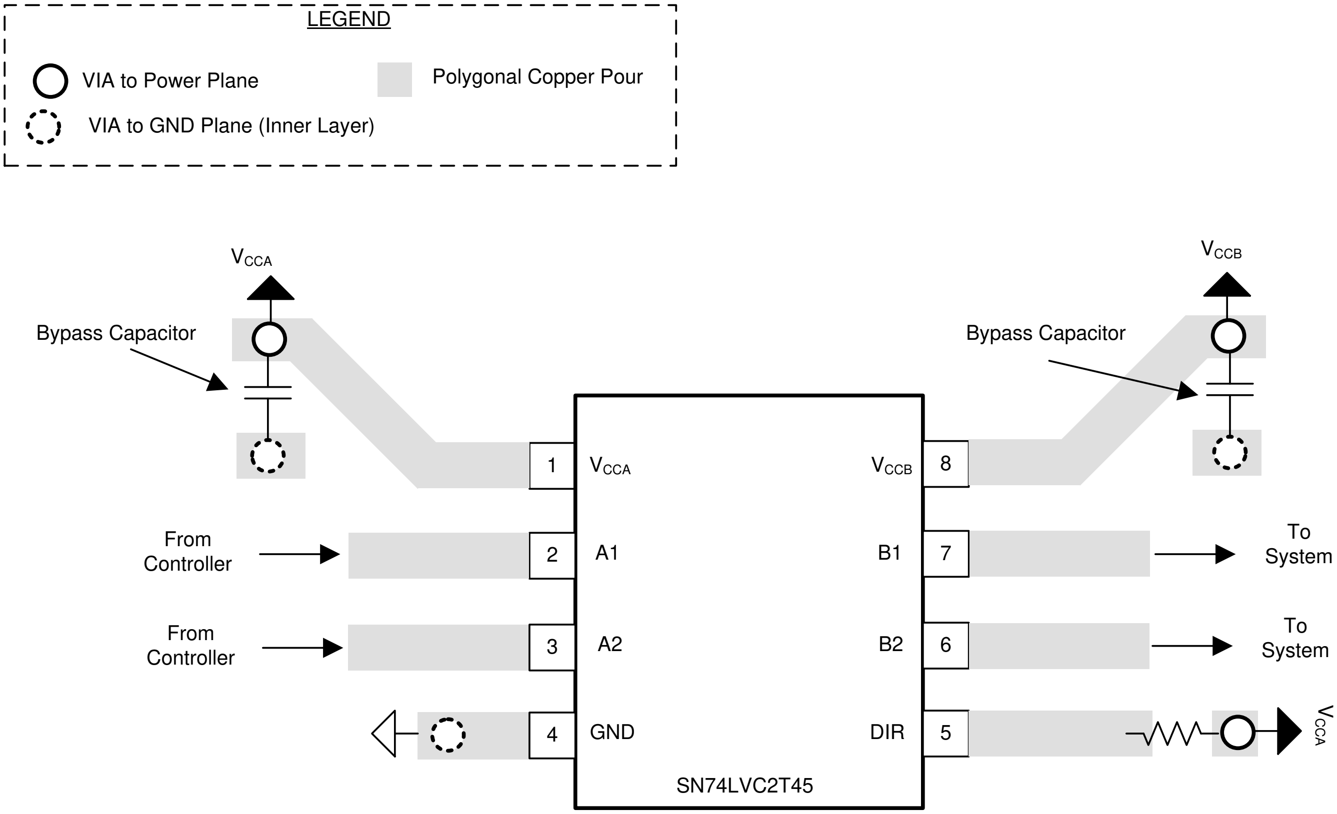

Figure 8-3. SN74LVC2T45 Layout Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction controlled voltage translators* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (October 2022) to Revision N (June 2024)	**Page**
• Updated the *Power Supply Recommendations* section	19

Changes from Revision L (October 2022) to Revision M (October 2022)	**Page**
• Changed the T_A *operating free-air temperature* back to *85°C*	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC2T45DCTR	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CT2 (R, Z)
SN74LVC2T45DCTR.A	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CT2 (R, Z)
SN74LVC2T45DCTRE4	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CT2 (R, Z)
SN74LVC2T45DCTT	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CT2 (R, Z)
SN74LVC2T45DCTT.A	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CT2 (R, Z)
SN74LVC2T45DCTTG4	Active	Production	SSOP (DCT) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	CT2 (R, Z)
SN74LVC2T45DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(CT2J, CT2Q, CT2R, T2) CZ
SN74LVC2T45DCUR.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(CT2J, CT2Q, CT2R, T2) CZ
SN74LVC2T45DCURE4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R
SN74LVC2T45DCURG4	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R
SN74LVC2T45DCURG4.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R
SN74LVC2T45DCUT	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(CT2J, CT2Q, CT2R, T2) CZ
SN74LVC2T45DCUT.A	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(CT2J, CT2Q, CT2R, T2) CZ
SN74LVC2T45DCUTG4	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R
SN74LVC2T45DCUTG4.A	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R
SN74LVC2T45DCUTG4.B	Active	Production	VSSOP (DCU) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CT2R
SN74LVC2T45YZPR	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TB, TB7)
SN74LVC2T45YZPR.B	Active	Production	DSBGA (YZP) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(TB, TB7)

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC2T45 :

- Automotive : SN74LVC2T45-Q1
- Enhanced Product : SN74LVC2T45-EP

NOTE: Qualified Version Definitions:

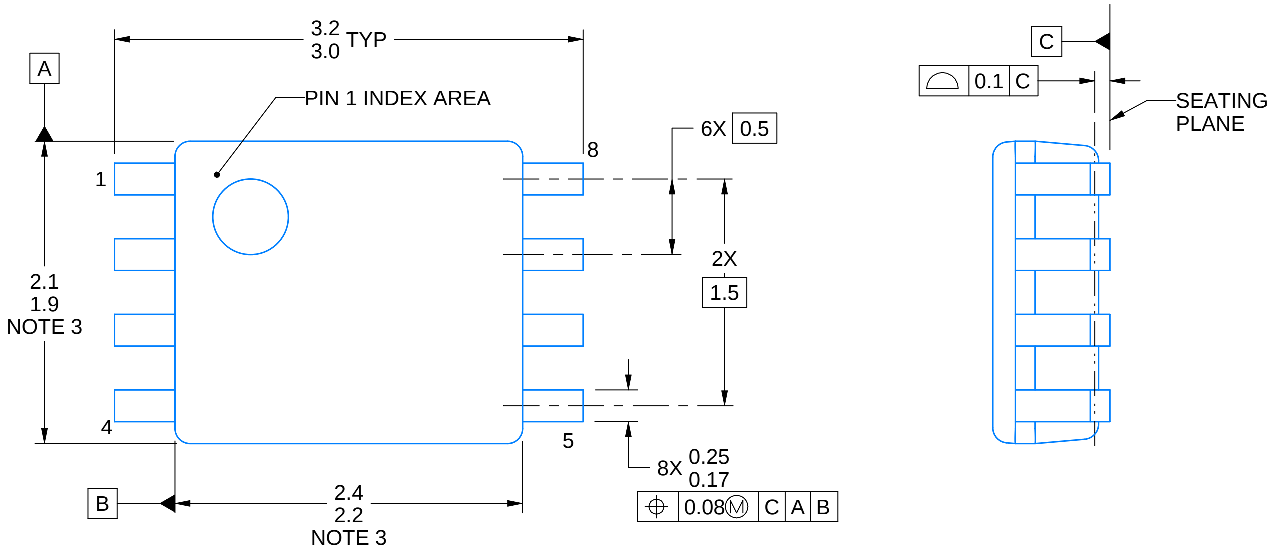
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

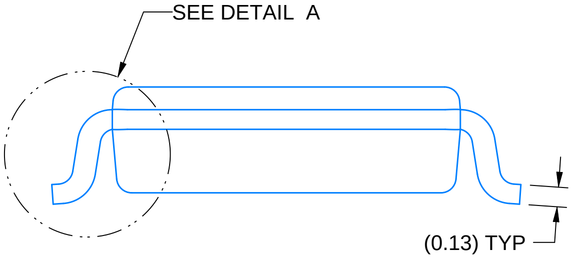
PACKAGE OUTLINE

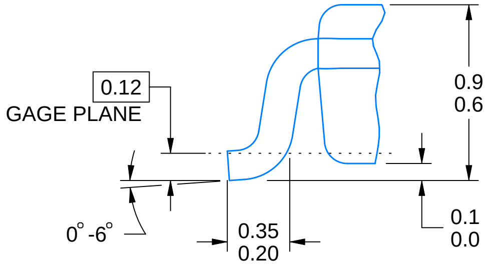
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE





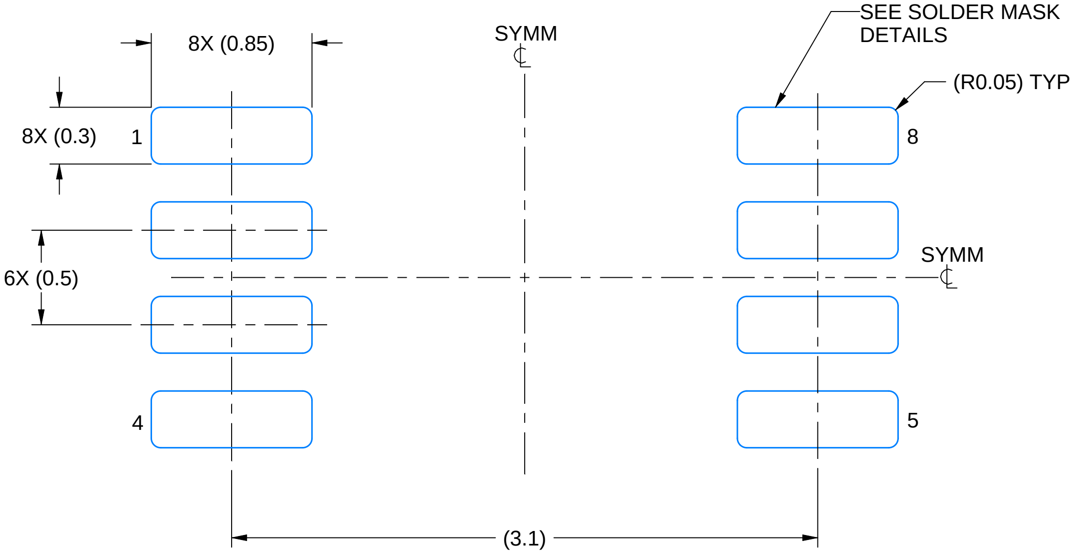


DETAIL A
TYPICAL

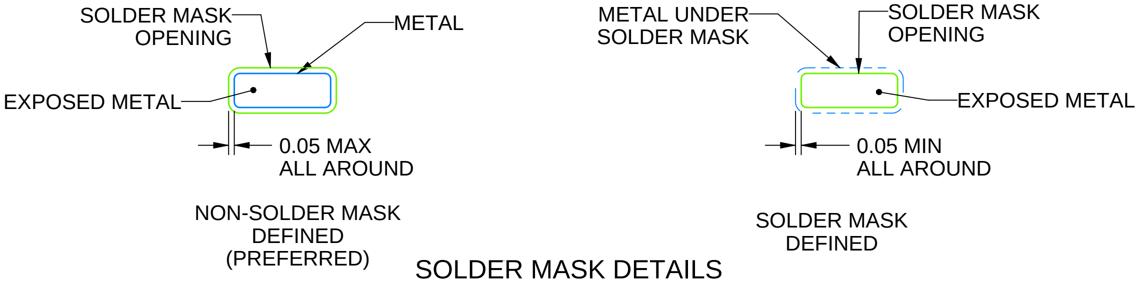
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

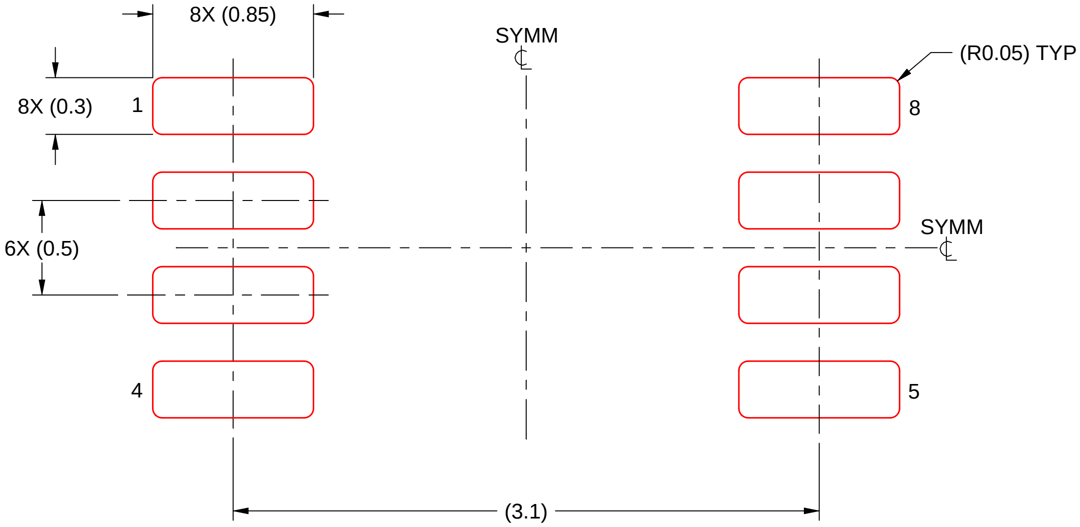


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



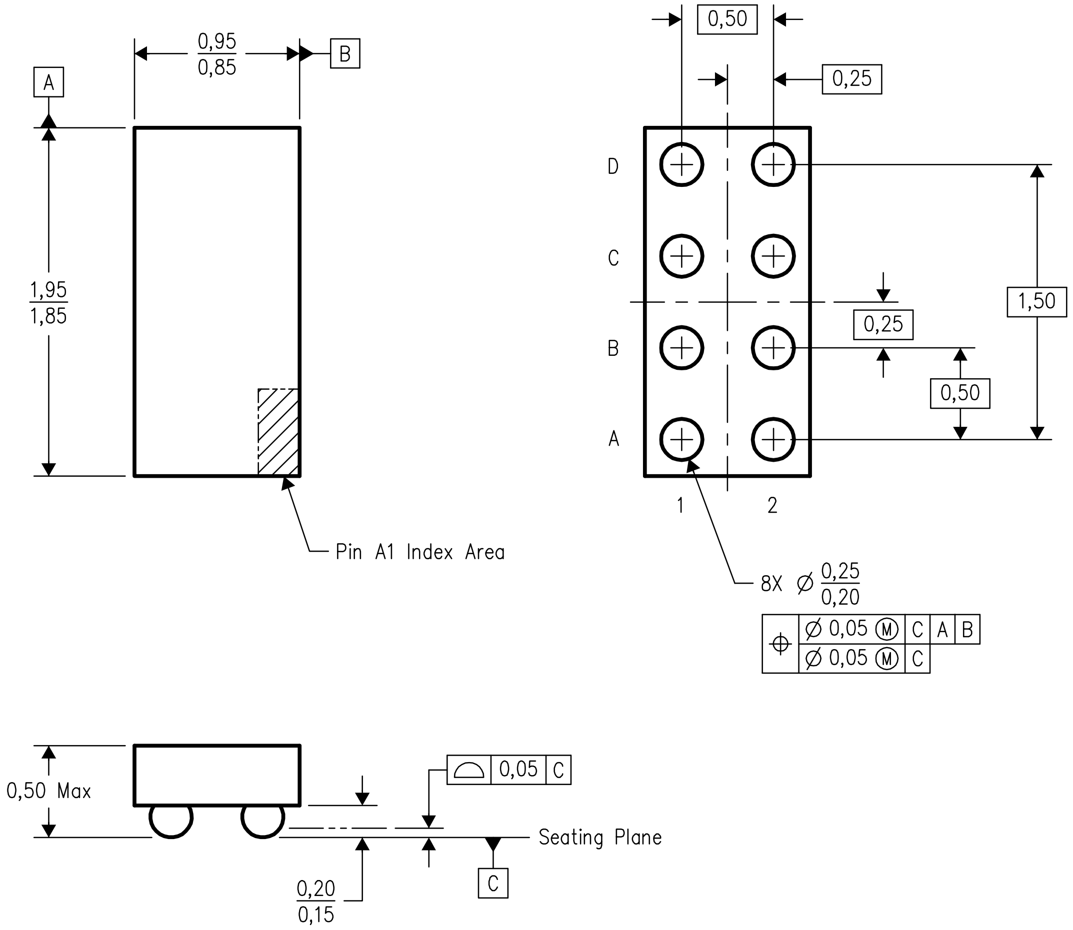
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

YEP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



4204725–4/A 10/2002

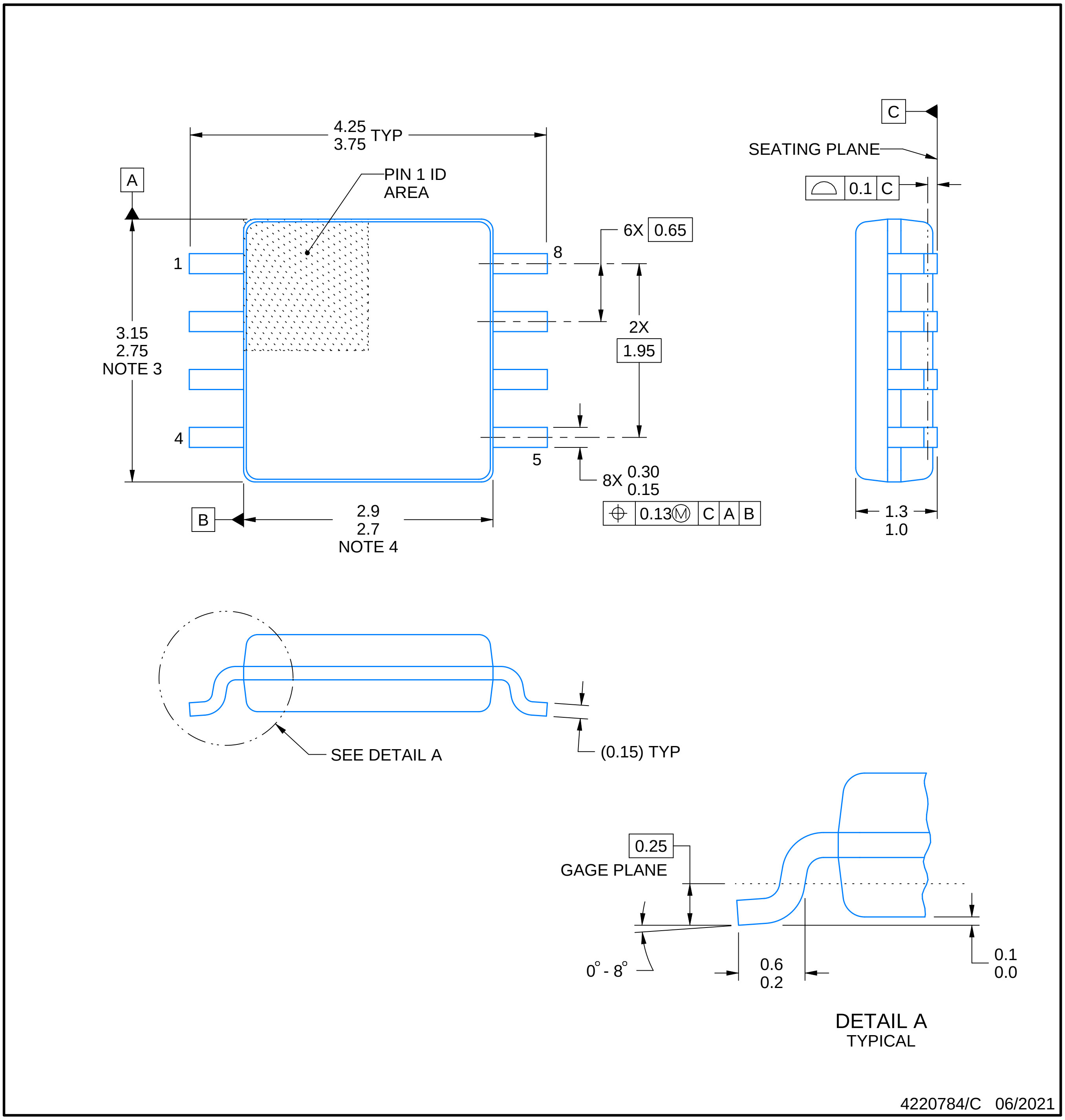
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. NanoStar™ package configuration.
- D. This package is tin–lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead–free.

NanoStar is a trademark of Texas Instruments.

PACKAGE OUTLINE

SSOP - 1.3 mm max height

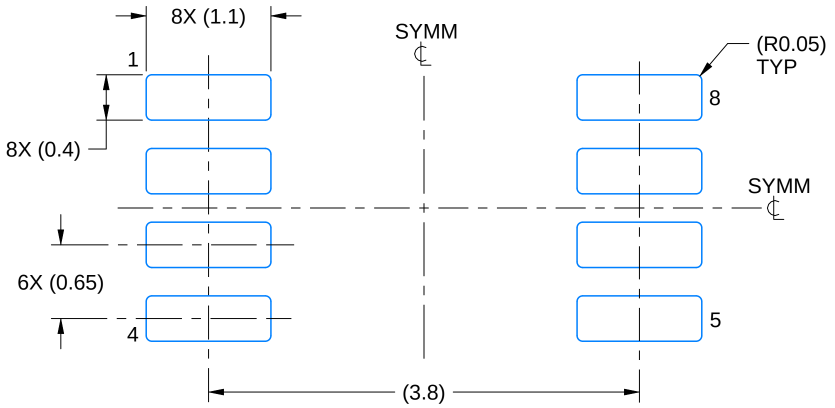
SMALL OUTLINE PACKAGE



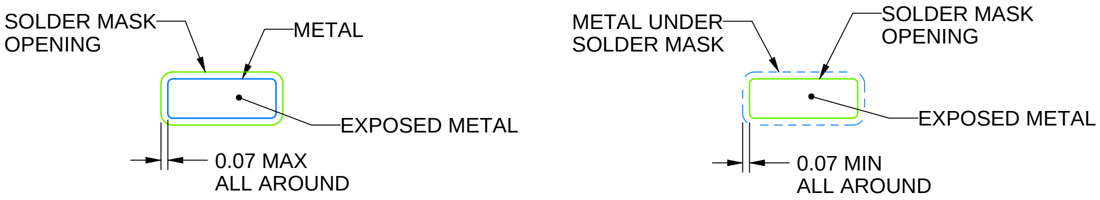
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



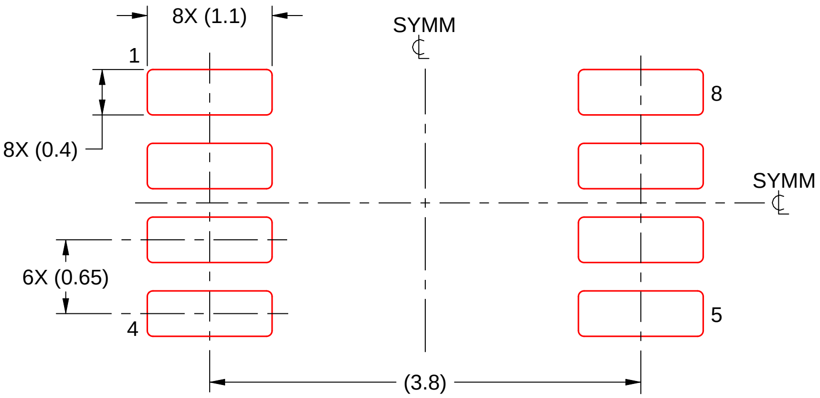
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

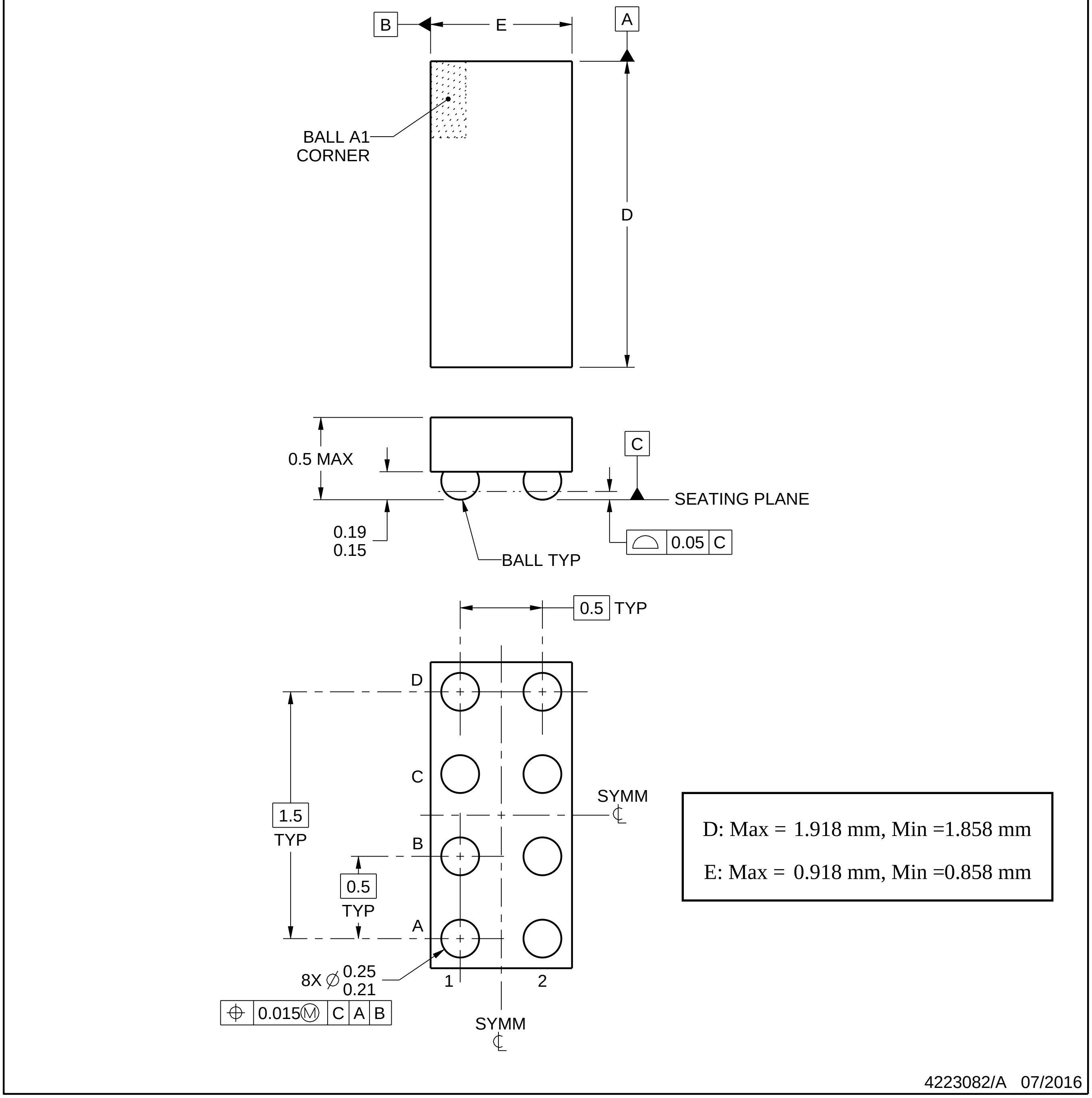
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

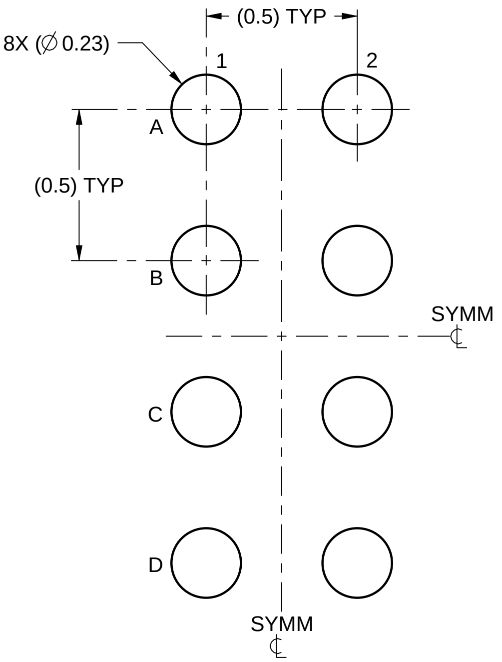


D: Max = 1.918 mm, Min =1.858 mm

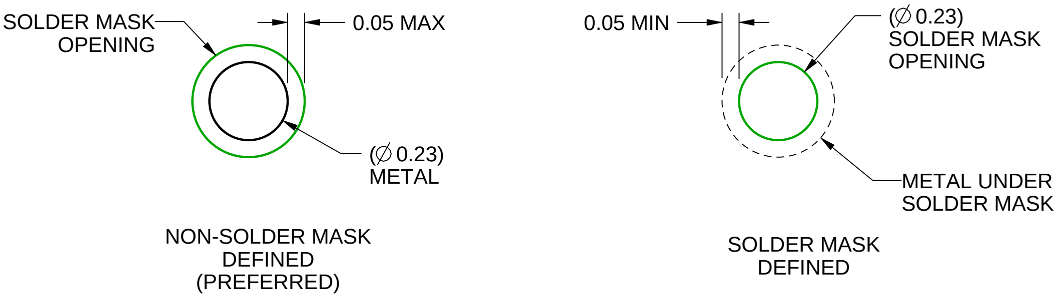
E: Max = 0.918 mm, Min =0.858 mm

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



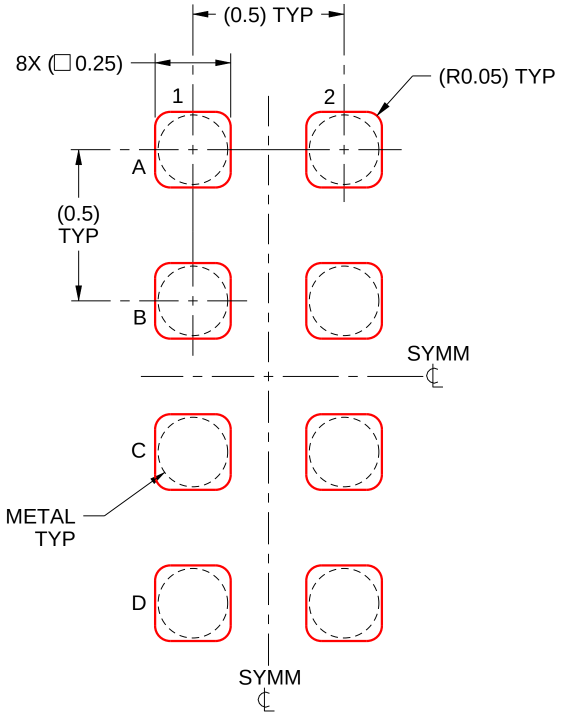
LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



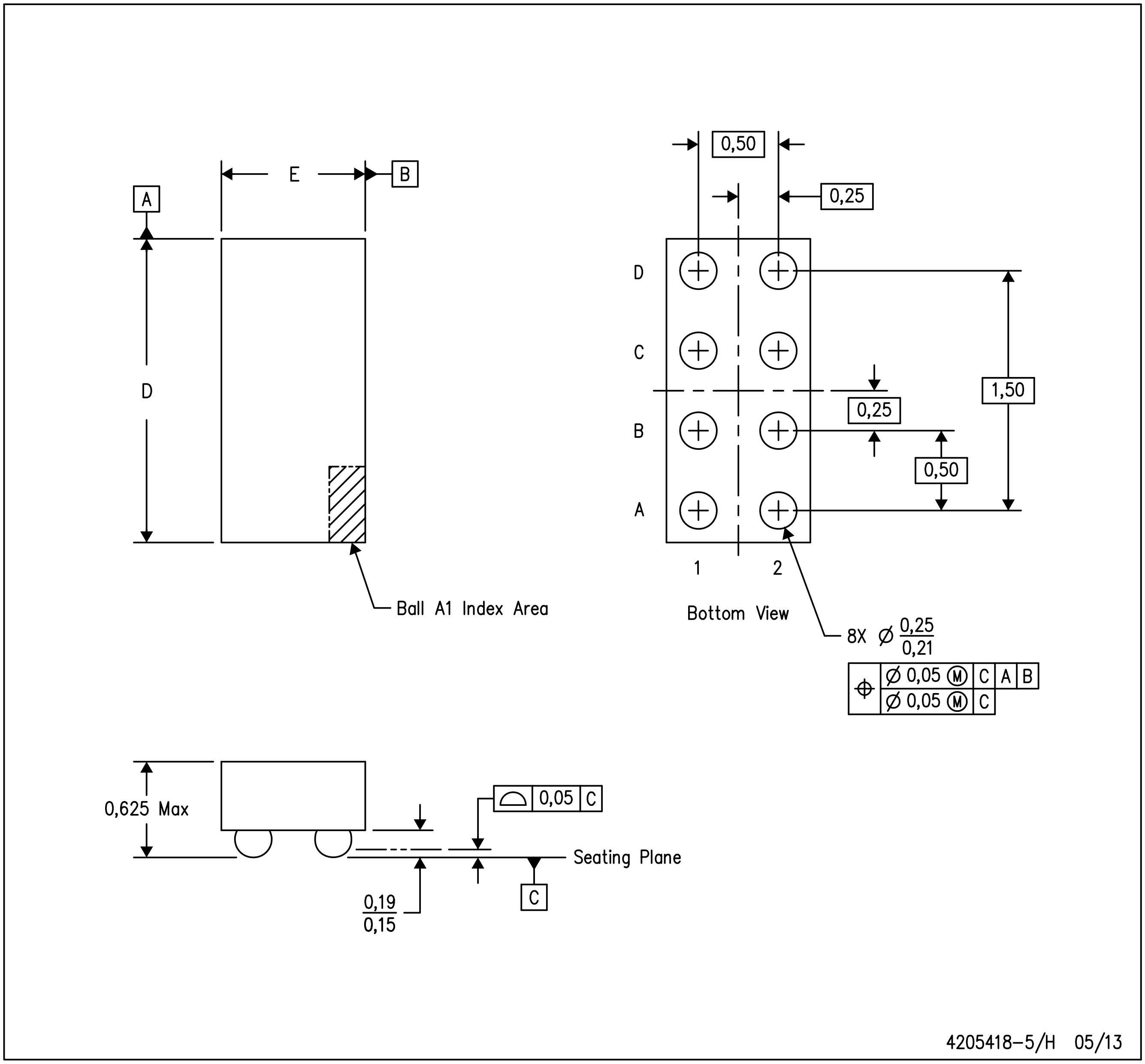
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZT (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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