SN74LVC126A Quadruple Bus Buffer Gate With 3-State Outputs

1 Features

- Operates from 1.65V to 3.6V
- Specified from –40°C to +125°C
- Inputs accept voltages up to 5.5V
- Maximum t_{pd} of 4.7ns at 3.3V
- Typical V_{OLP} (output ground bounce), <0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot), >2V at V_{CC} = 3.3V, T_A = 25°C
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theaters
- MP3 Players or Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom, Server, and AC-DC Supplies (Single-Controller, Analog, and Digital)
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description

The SN74LVC126A device is a quadruple bus buffer gate designed for 1.65V to 3.6V V_{CC} operation.

The SN74LVC126A device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

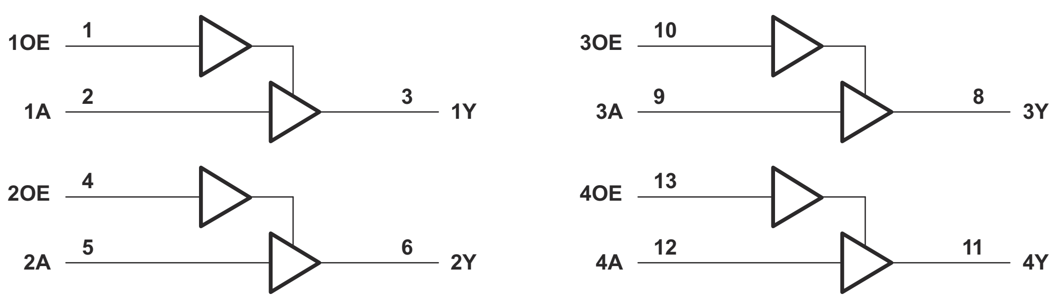
To ensure the high-impedance state during power up or power down, OE must be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V and 5V system environment.

Package Information

PART NUMBER	PACKAGE [1]	PACKAGE SIZE[2]	BODY SIZE[3]
SN74LVC126A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.65mm x 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.2mm x 7.8mm	6.20mm × 5.30mm
	DGV (TVSOP, 14)	3.60mm × 6.4mm	3.60mm × 4.40mm
	NS (SOP, 14)	10.2mm x 7.8mm	10.20mm × 5.30mm
	PW (TSSOP, 14)	5mm x 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm	3.50mm × 3.50mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic

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4 Pin Configuration and Functions

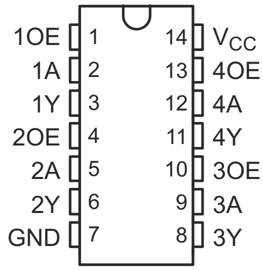


Figure 4-1. SN74LVC126A D, DB, DGV, NS, or PW Package; 14-Pin SOIC, SSOP, TVSOP, SOP or TSSOP (Top View)

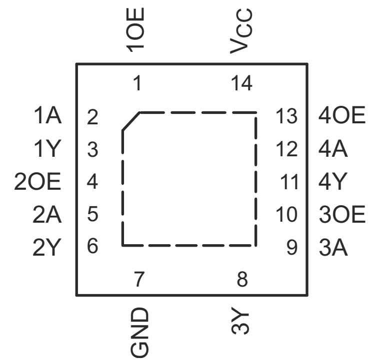


Figure 4-2. SN74LVC126A BQA or RGY Package;14-Pin WQFN or VQFN (Top View)

Table 4-1. Pin Functions

PIN		I/O[(1)]	DESCRIPTION
NO.	NAME		
1	1OE	I	Output enable 1
2	1A	I	Gate 1 input
3	1Y	O	Gate 1 output
4	2OE	I	Output enable 2
5	2A	I	Gate 2 input
6	2Y	O	Gate 2 output
7	GND	—	Ground pin
8	3Y	O	Gate 3 output
9	3A	I	Gate 3 input
10	3OE	I	Output enable 3
11	4Y	O	Gate 4 output
12	4A	I	Gate 4 input
13	4OE	I	Output Enable 4
14	V_{CC}	—	Power pin
Thermal pad		—	Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I [2]	Input voltage		–0.5	6.5	V
V_O [2] [3]	Output voltage		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
P_{tot}	Power dissipation	T_A = –40°C to +125°C[4] [5]		500	mW
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in *Recommended Operating Conditions*.
(4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
(5) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. This rating was tested on the D (SOIC) package.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. This rating was tested on the D (SOIC) package.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65		3.6	V
		Data retention only	1.5			
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}			V
		V_{CC} = 2.3 V to 2.7 V	1.7			
		V_{CC} = 2.7 V to 3.6 V	2			
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V			0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7	
		V_{CC} = 2.7 V to 3.6 V			0.8	
V_I	Input voltage		0		5.5	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V			–4	mA
		V_{CC} = 2.3 V			–8	
		V_{CC} = 2.7 V			–12	
		V_{CC} = 3 V			–24	

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	NOM	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 1.65 V			4	mA
		V_{CC} = 2.3 V			8	
		V_{CC} = 2.7 V			12	
		V_{CC} = 3 V			24	
Δt/Δv	Input transition rise or fall rate				10	ns/V
T_A	Operating free-air temperature		–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

THERMAL METRIC[(1)]		SN74LVC126A							UNIT
		BQA (WQFN)	D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.3[(3)]	127.8[(2)]	112.2[(2)]	140.9[(2)]	123.8[(2)]	150.8[(2)]	92.1[(3)]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.8	81.9	64.2	59.9	51.7	78.3	91.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	84.4	59.6	70.2	52.7	93.8	66.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.6	39.6	28.3	9.1	20.7	38.2	20	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.9	83.9	59.1	69.5	52.3	93.2	66.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	50.1	N/A	N/A	N/A	N/A	N/A	50.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) The package thermal impedance is calculated in accordance with JESD 51-5.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 µA, V_{CC} = 1.65 V to 3.6 V		T_A = 25°C	V_{CC} – 0.2			V
			T_A = –40°C to +125°C	V_{CC} – 0.3			
	I_{OH} = –4 mA, V_{CC} = 1.65 V		T_A = 25°C	1.29			
			T_A = –40°C to +85°C	1.2			
			T_A = –40°C to +125°C	1.05			
	I_{OH} = –8 mA, V_{CC} = 2.3 V		T_A = 25°C	1.9			
			T_A = –40°C to +85°C	1.7			
			T_A = –40°C to +125°C	1.55			
	I_{OH} = –12 mA	V_{CC} = 2.7 V	T_A = 25°C	2.2			
			T_A = –40°C to +125°C	2.05			
		V_{CC} = 3 V	T_A = 25°C	2.4			
			T_A = –40°C to +125°C	2.25			
	I_{OH} = –24 mA, V_{CC} = 3 V		T_A = 25°C	2.3			
			T_A = –40°C to +85°C	2.2			
			T_A = –40°C to +125°C	2			
V_{OL}	I_{OL} = 100 µA, V_{CC} = 1.65 V to 3.6 V		T_A = 25°C			0.1	V
			T_A = –40°C to +85°C			0.2	
			T_A = –40°C to +125°C			0.3	
	I_{OL} = 4 mA, V_{CC} = 1.65 V		T_A = 25°C			0.24	
			T_A = –40°C to +85°C			0.45	
			T_A = –40°C to +125°C			0.6	
	I_{OL} = 8 mA, V_{CC} = 2.3 V		T_A = 25°C			0.3	
			T_A = –40°C to +85°C			0.7	
			T_A = –40°C to +125°C			0.75	
	I_{OL} = 12 mA, V_{CC} = 2.7 V		T_A = 25°C			0.4	
			T_A = –40°C to +125°C			0.6	
	I_{OL} = 24 mA, V_{CC} = 3 V		T_A = 25°C			0.55	
			T_A = –40°C to +125°C			0.8	
I_I	V_I = 5.5 V or GND, V_{CC} = 3.6 V		T_A = 25°C			±1	µA
			T_A = –40°C to +85°C			±5	
			T_A = –40°C to +125°C			±20	
I_{OZ}	V_O = V_{CC} or GND, V_{CC} = 3.6 V		T_A = 25°C			±1	µA
			T_A = –40°C to +85°C			±10	
			T_A = –40°C to +125°C			±20	
I_{CC}	V_I = V_{CC} or GND, I_O = 0, V_{CC} = 3.6 V		T_A = 25°C			1	µA
			T_A = –40°C to +85°C			10	
			T_A = –40°C to +125°C			40	
ΔI_{CC}	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND, V_{CC} = 2.7 V to 3.6 V		T_A = 25°C			500	µA
			T_A = –40°C to +125°C			5000	
C_i	V_I = V_{CC} or GND, V_{CC} = 3.3 V				4.5		pF
C_o	V_O = V_{CC} or GND, V_{CC} = 3.3 V				7		pF

5.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	f = 10 MHz, T_A = 25°C	Outputs enabled	V_{CC} = 1.8 V		20		pF
				V_{CC} = 2.5 V		21		
				V_{CC} = 3.3 V		22		
			Outputs disabled	V_{CC} = 1.8 V		2		
				V_{CC} = 2.5 V		3		
				V_{CC} = 3.3 V		4		

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted; see *Parameter Measurement Information*)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{pd}	From A (input) to Y (output)	V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	1	4.2	9.3	ns
			T_A = –40°C to +85°C			9.8	
			T_A = –40°C to +125°C			11.3	
		V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	1	2.7	6.7	
			T_A = –40°C to +85°C			7.2	
			T_A = –40°C to +125°C			9.3	
		V_{CC} = 2.7 V	T_A = 25°C	1	2.9	5	
			T_A = –40°C to +85°C			5.2	
			T_A = –40°C to +125°C			6.5	
		V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	1	2.5	4.5	
			T_A = –40°C to +85°C			4.7	
			T_A = –40°C to +125°C			6	
t_{en}	From OE (input) to Y (output)	V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	1	4.8	9.5	ns
			T_A = –40°C to +85°C			10	
			T_A = –40°C to +125°C			11.5	
		V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	1	2.8	7.8	
			T_A = –40°C to +85°C			8.3	
			T_A = –40°C to +125°C			10.4	
		V_{CC} = 2.7 V	T_A = 25°C	1	3.1	6.1	
			T_A = –40°C to +85°C			6.3	
			T_A = –40°C to +125°C			8	
		V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	1	2.5	5.5	
			T_A = –40°C to +85°C			5.7	
			T_A = –40°C to +125°C			7.5	

5.6 Switching Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted; see *Parameter Measurement Information*)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{dis}	From OE (input) to Y (output)	V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	1	4.4	12.1	ns
			T_A = –40°C to +85°C			12.6	
			T_A = –40°C to +125°C			14.1	
		V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	1	2.7	8.2	
			T_A = –40°C to +85°C			8.7	
			T_A = –40°C to +125°C			10.8	
		V_{CC} = 2.7 V	T_A = 25°C	1	2.7	6.5	
			T_A = –40°C to +85°C			6.7	
			T_A = –40°C to +125°C			8.5	
		V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	1.3	2.3	5.8	
			T_A = –40°C to +85°C			6	
			T_A = –40°C to +125°C			7.5	
$t_{sk(o)}$	V_{CC} = 3.3 V ± 0.3 V		T_A = –40°C to +85°C			1	ns
			T_A = –40°C to +125°C			1.5	

5.7 Typical Characteristics

T_A = 25°C

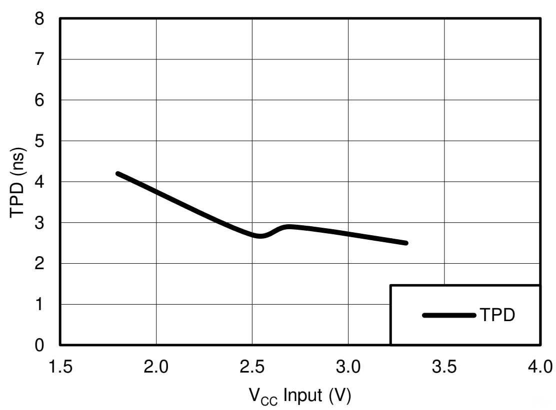


Figure 5-1. TPD vs V_{CC}

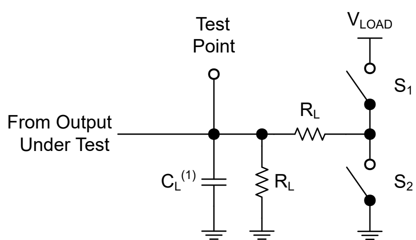
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

The outputs are measured individually with one input transition per measurement.

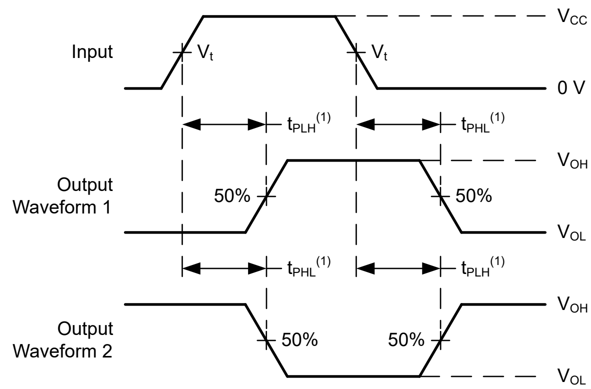
TEST	S1	S2	R_L	C_L	ΔV	V_{LOAD}
t_{PLH}, t_{PHL}	OPEN	OPEN	500Ω	50pF	—	—
t_{PLZ}, t_{PZL}	CLOSED	OPEN	500Ω	50pF	0.3V	2×V_{CC}
t_{PHZ}, t_{PZH}	OPEN	CLOSED	500Ω	50pF	0.3V	—

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V	2×V_{CC}
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V	2×V_{CC}
2.7V	1.5V	500Ω	50pF	0.3V	6V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V	6V



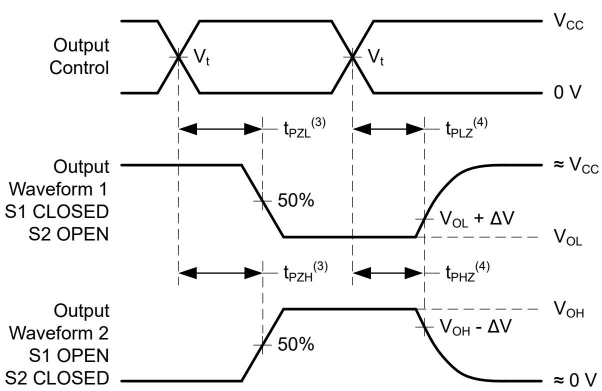
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

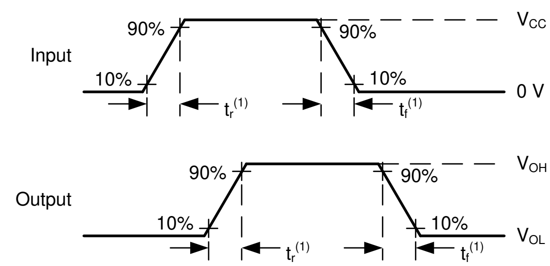
Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

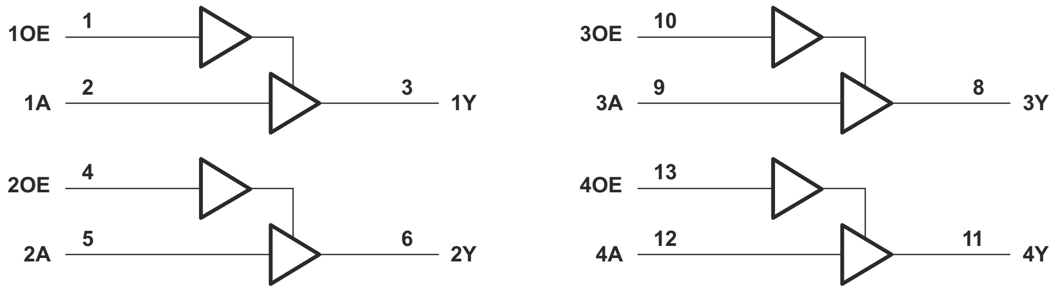
7.1 Overview

The SN74LVC126A quadruple buffer is designed for 1.65-V to 3.6-V V_{CC} operation and features tri-state outputs.

The SN74LVC126A devices perform the Boolean function Y = A in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as down-translators in a mixed 3.3-V or 5-V system environment.

7.2 Functional Block Diagram



7.3 Feature Description

The SN74LVC126A device features four independent buffers with 3-state outputs, and is designed to operate from a V_{CC} of 1.65 V to 3.6 V. When the output enable (OE) input is low, the corresponding output is disabled and enters a high-impedance state. This device also features high-tolerance inputs, allowing for voltage translation in mixed voltage systems. Wide operating temperature range enables this device to be used in any application, including rugged or extreme environments.

7.4 Device Functional Modes

The SN74LVC126A's 3-state outputs allow the outputs to be disabled using the output enable (OE) pin. To ensure the high-impedance state during power up and power down, OE must be tied to GND through a pulldown resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

Table 7-1. Function Table (Each Buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Hi-Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC126A device is a high-drive, CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 MHz. The inputs and outputs are 5.5-V tolerant allowing the device to translate up to 5.5 V or down to V_{CC}.

8.2 Typical Application

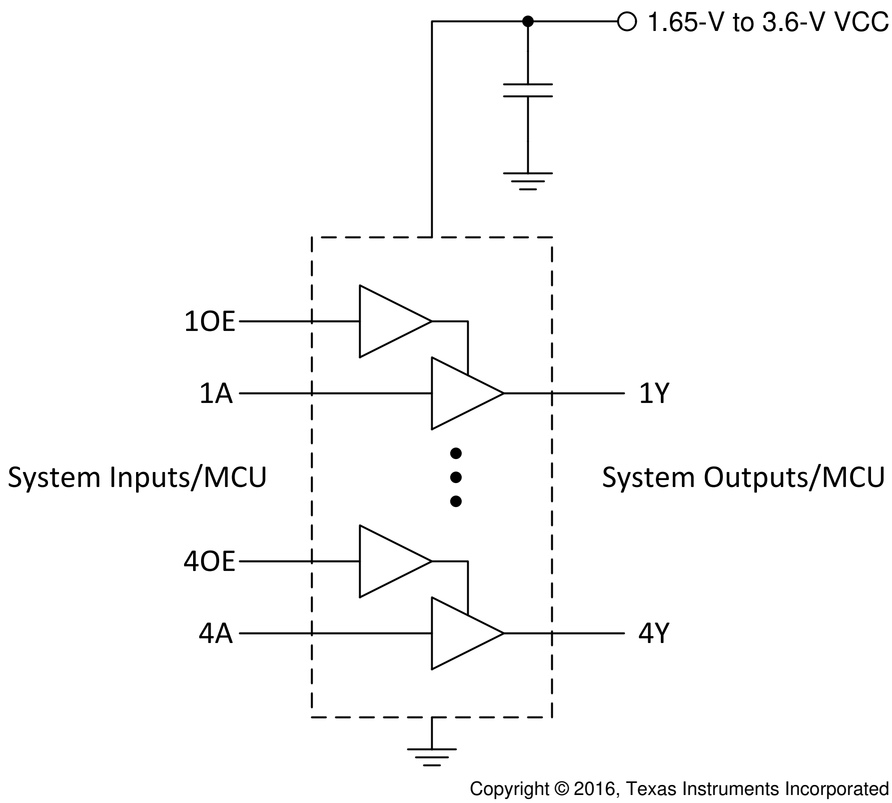


Figure 8-1. Typical Buffer Application and Supply Voltage

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads; therefore, routing and load conditions must be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specifications: See (Δt/ΔV) in *Recommended Operating Conditions.*
   - Specified high and low levels: See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions
   - Load currents must not exceed 25 mA per output and 50 mA total for the part.
   - Outputs must not be pulled above 5.5 V.

8.2.3 Application Curve

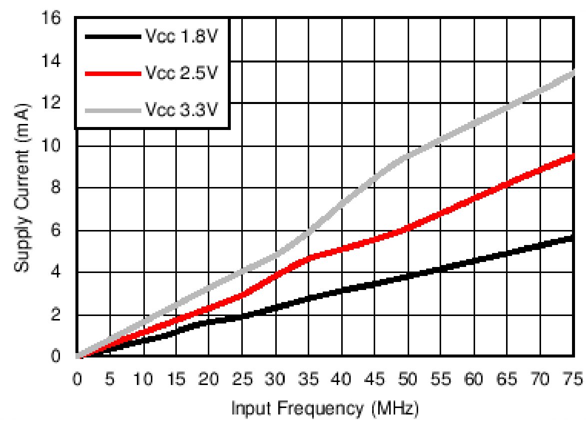


Figure 8-2. Supply Current vs Input Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating in the *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 8-3 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

8.4.2 Layout Example

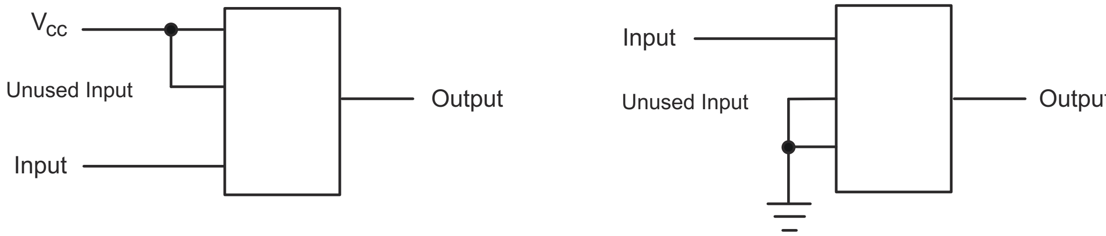


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision T (May 2024) to Revision U (July 2024) **Page**

- Updated RθJA values: D = 98.4 to 127.8, NS = 93.9 to 123.8, PW = 127.7 to 150.8, RGY = 35 to 92.1; Updated D, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W 5

Changes from Revision S (February 2017) to Revision T (May 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added BQA package to *Package Information* table, *Pin Configuration and Functions* section, and *Thermal Information* table.. 1
- Added package size to *Package Information* table.. 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC126ABQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LVC126ABQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LVC126AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126AD.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADBR.B	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADGVR	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADGVR.B	Active	Production	TVSOP (DGV) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADT	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ADT.B	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ANSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ANSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126ANSR.B	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC126A
SN74LVC126APW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWG4	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWRE4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A
SN74LVC126APWT.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC126A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC126ARGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A
SN74LVC126ARGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A
SN74LVC126ARGYR.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A
SN74LVC126ARGYRG4	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC126A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC126A :

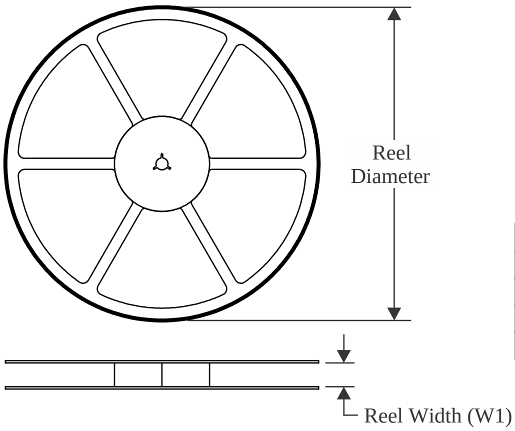
- Automotive : SN74LVC126A-Q1

NOTE: Qualified Version Definitions:

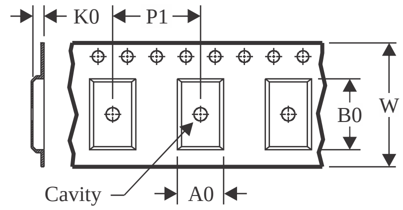
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

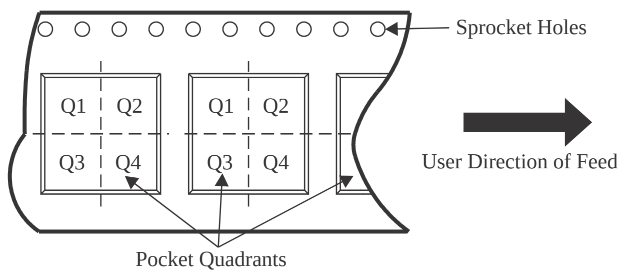


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

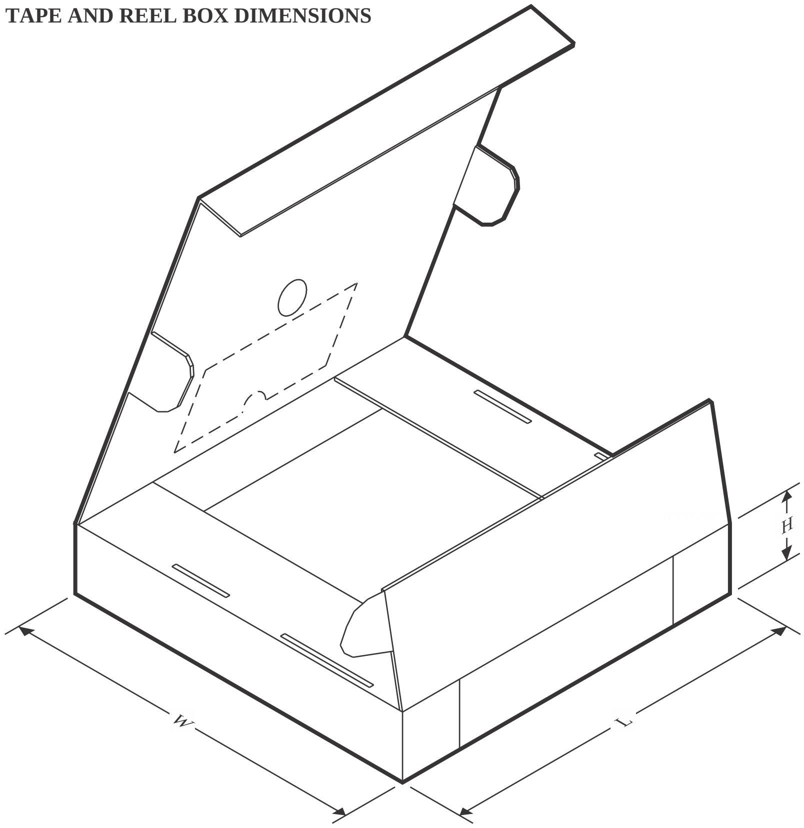
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC126ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC126ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC126ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC126ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC126APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC126APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC126ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

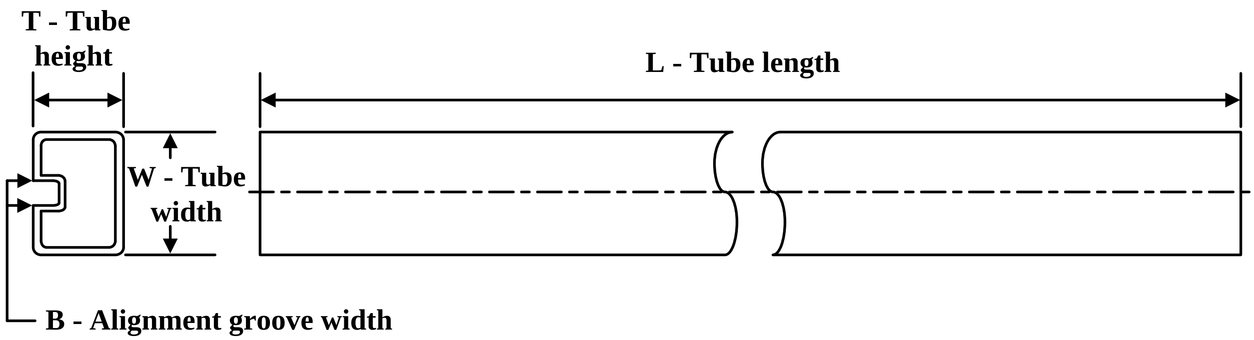
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC126ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC126ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC126ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LVC126ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC126ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC126ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LVC126APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC126APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LVC126ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC126AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC126AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC126APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC126APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC126APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

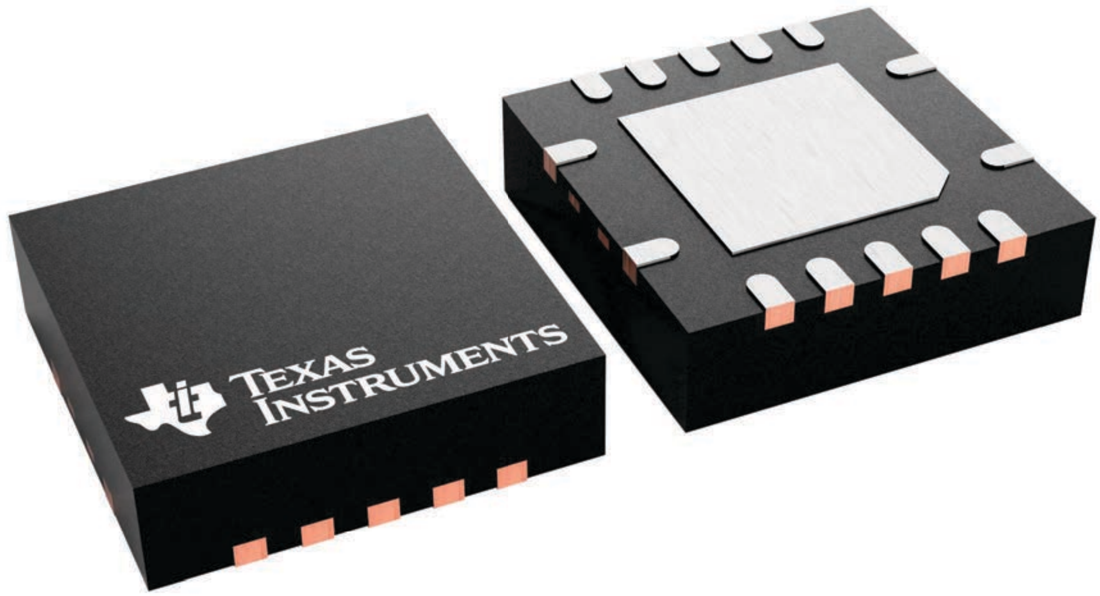
GENERIC PACKAGE VIEW

RGY 14 | **VQFN - 1 mm max height**

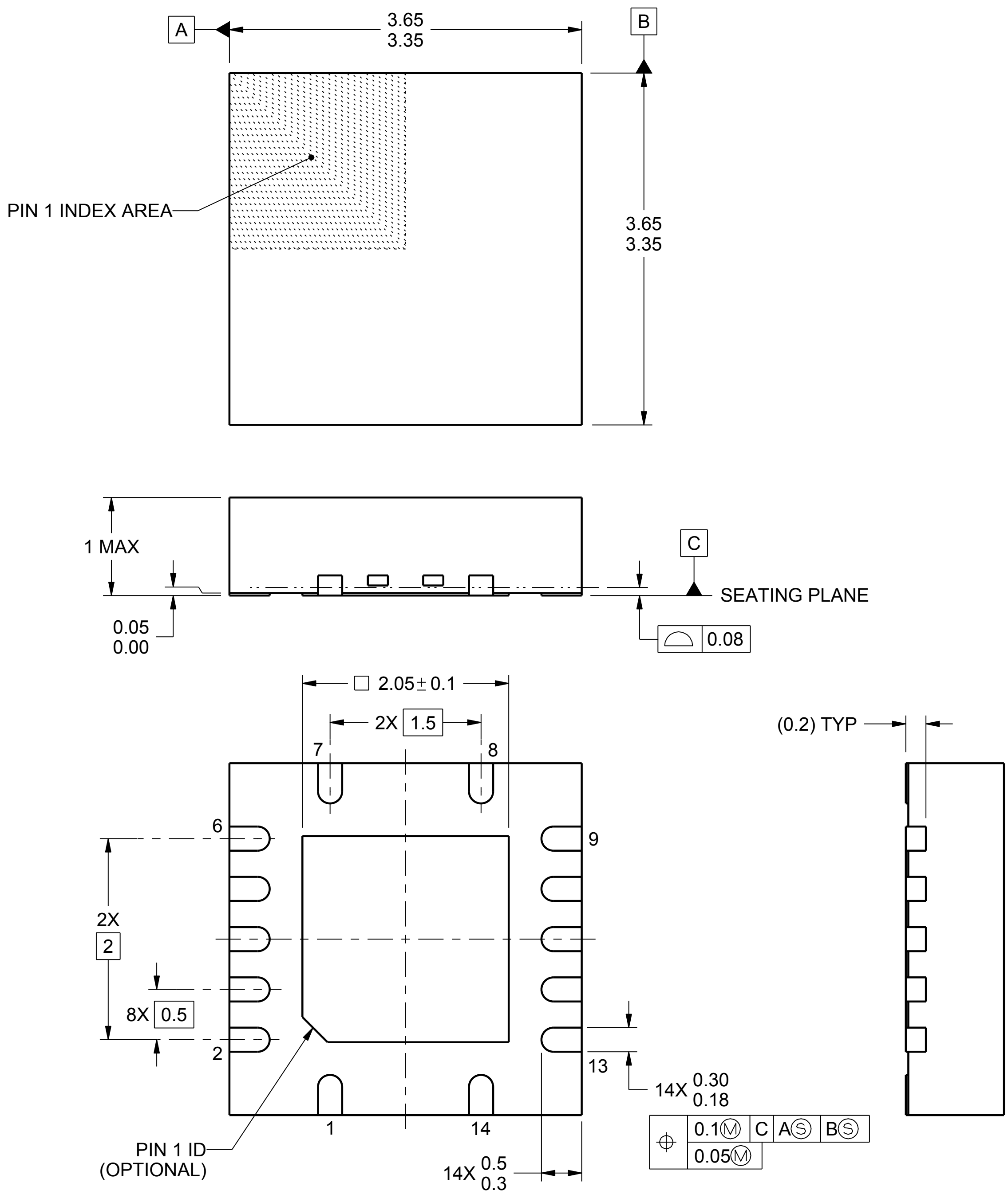
3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



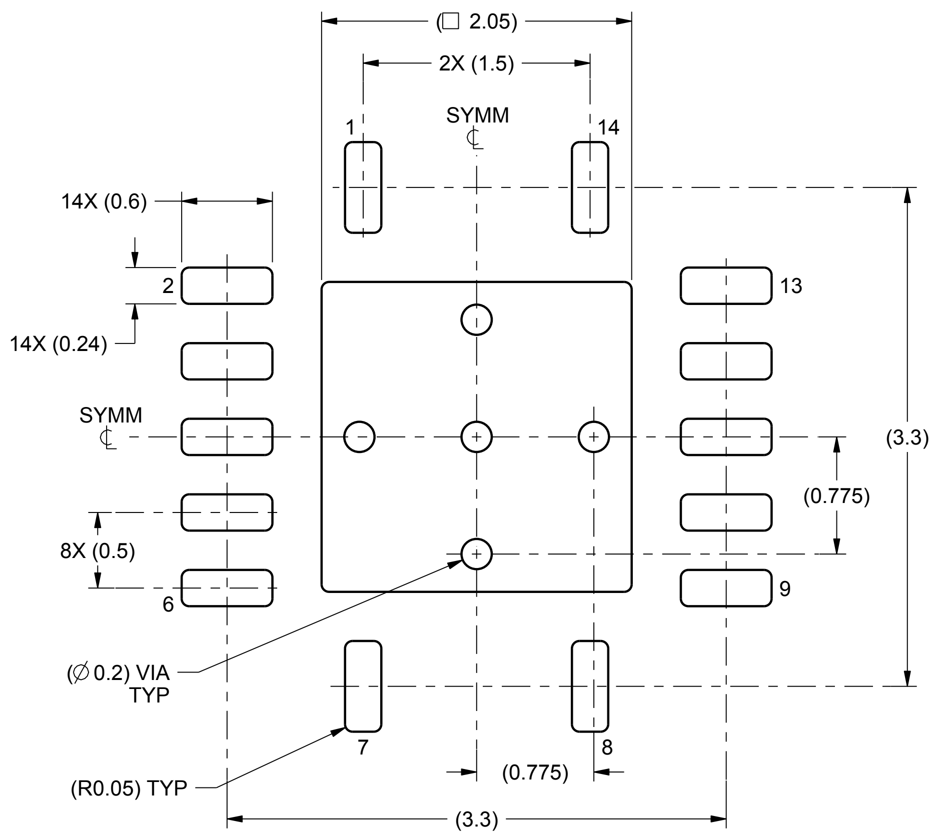
4231541/A



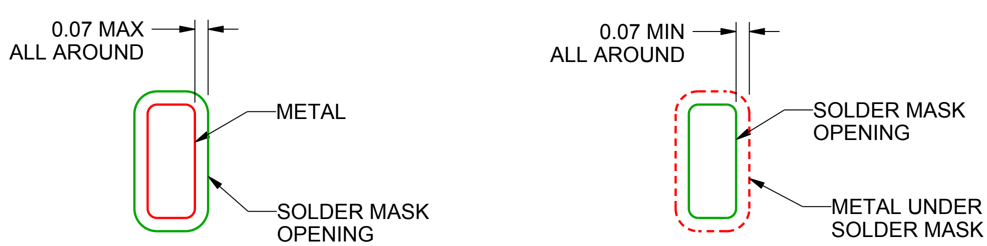
4219040/A 09/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

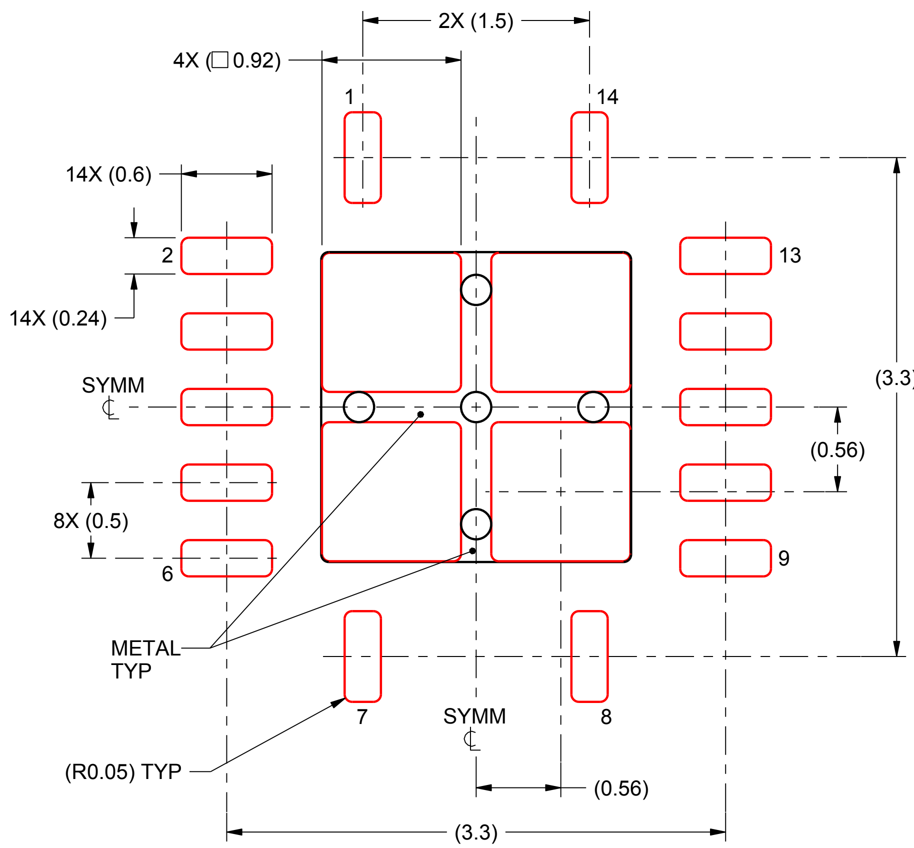
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



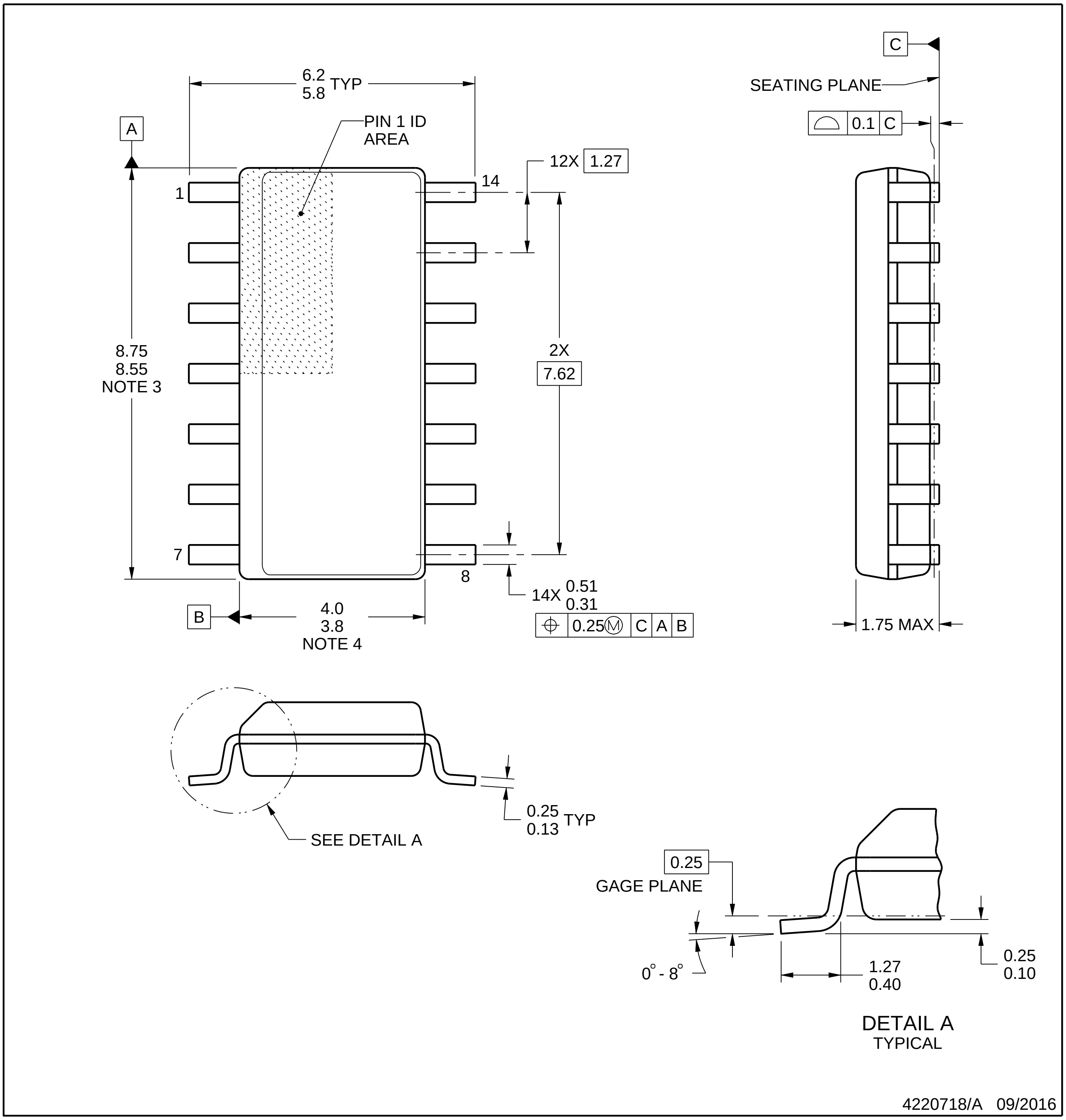
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

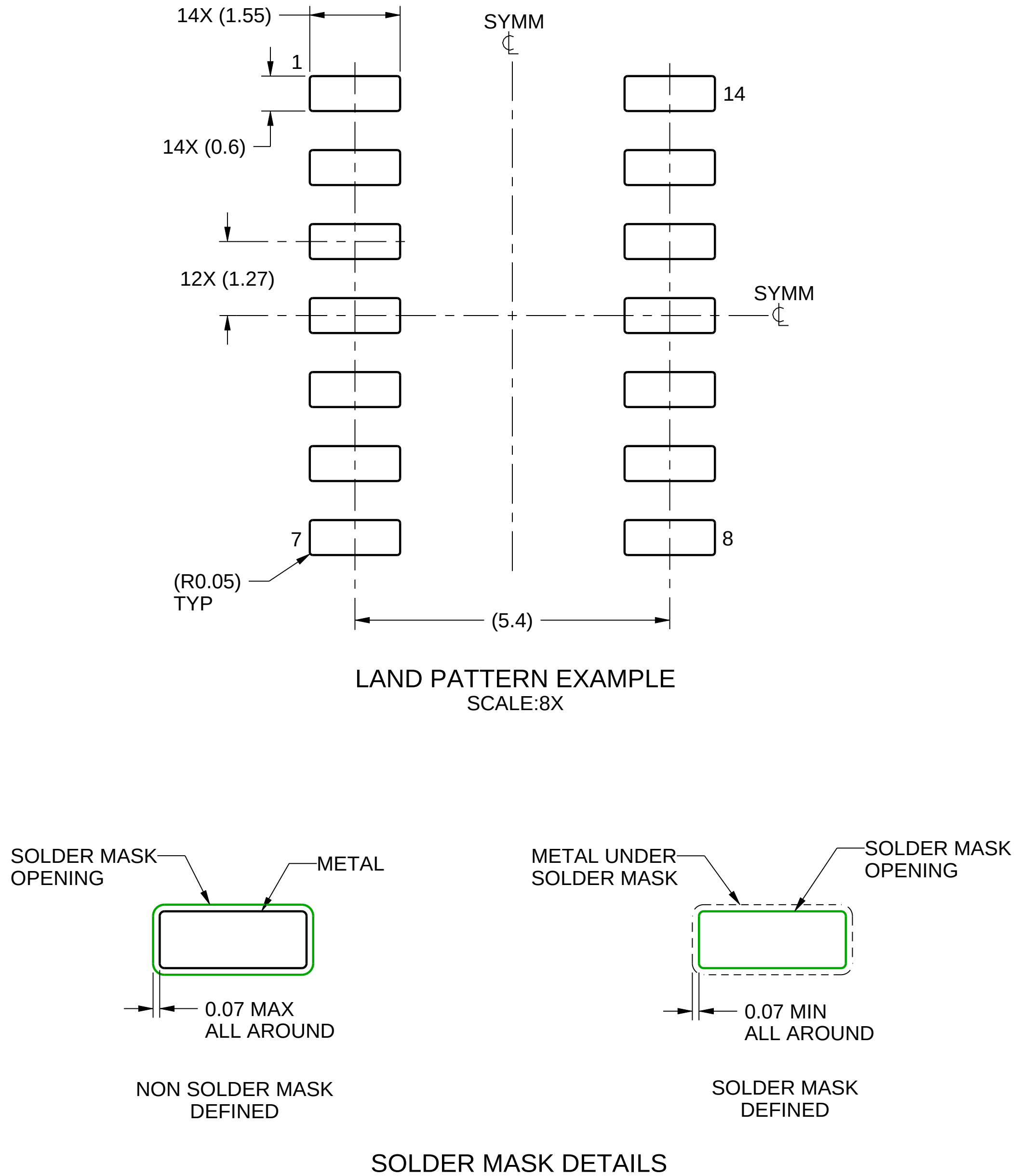
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



NOTES:

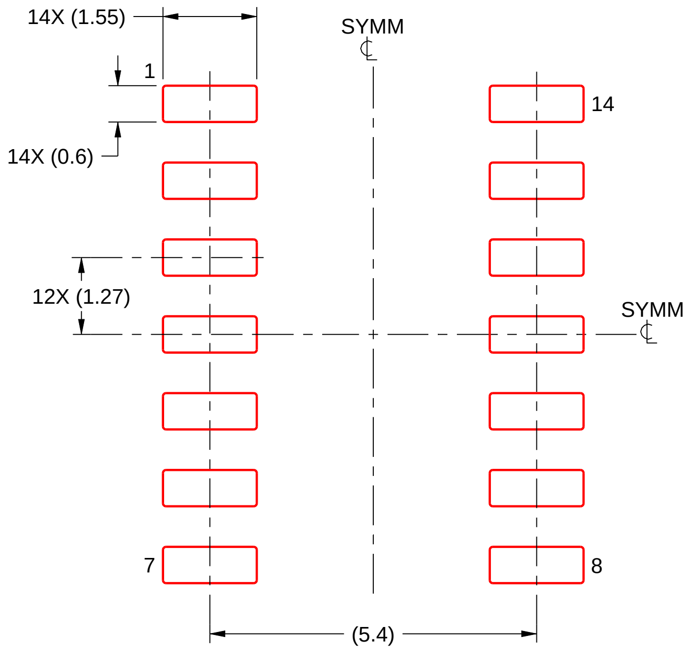
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

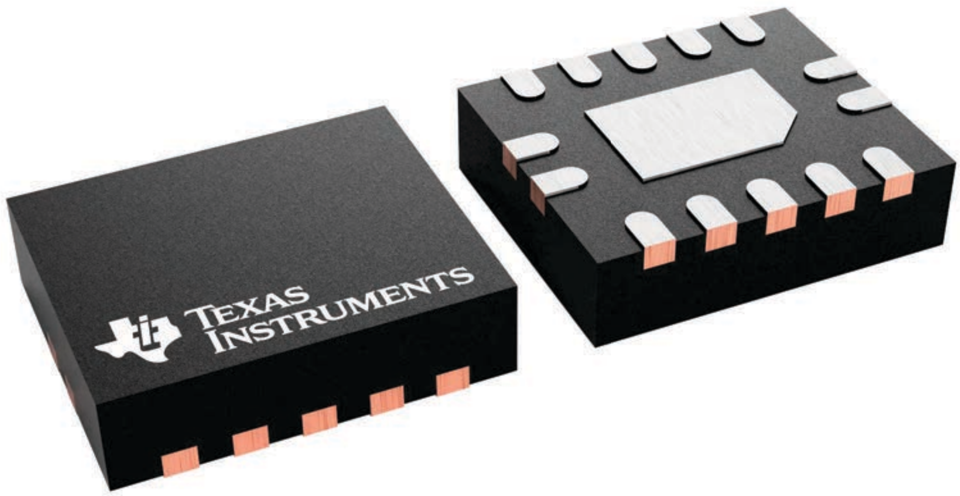
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

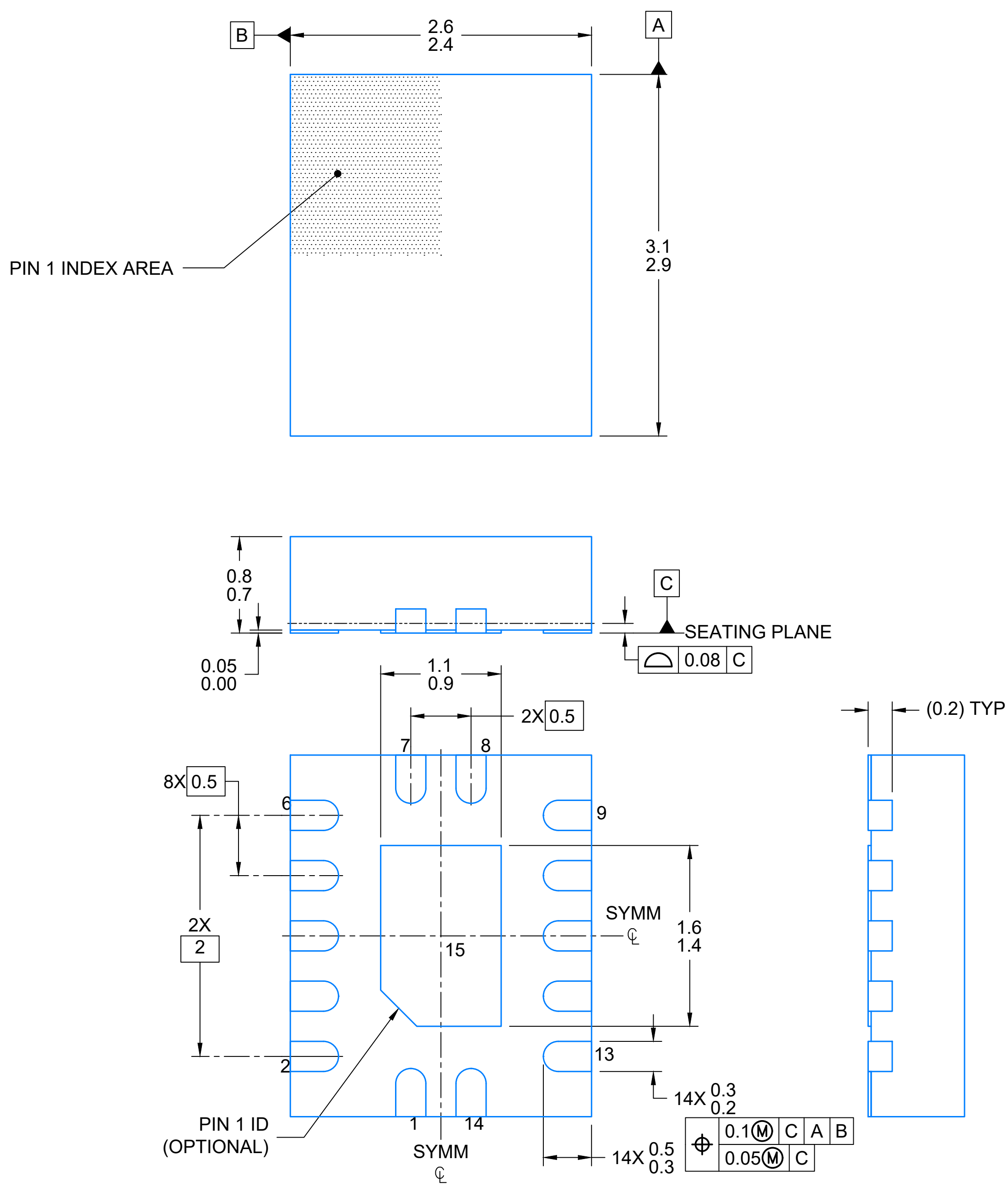
BQA 14 **WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



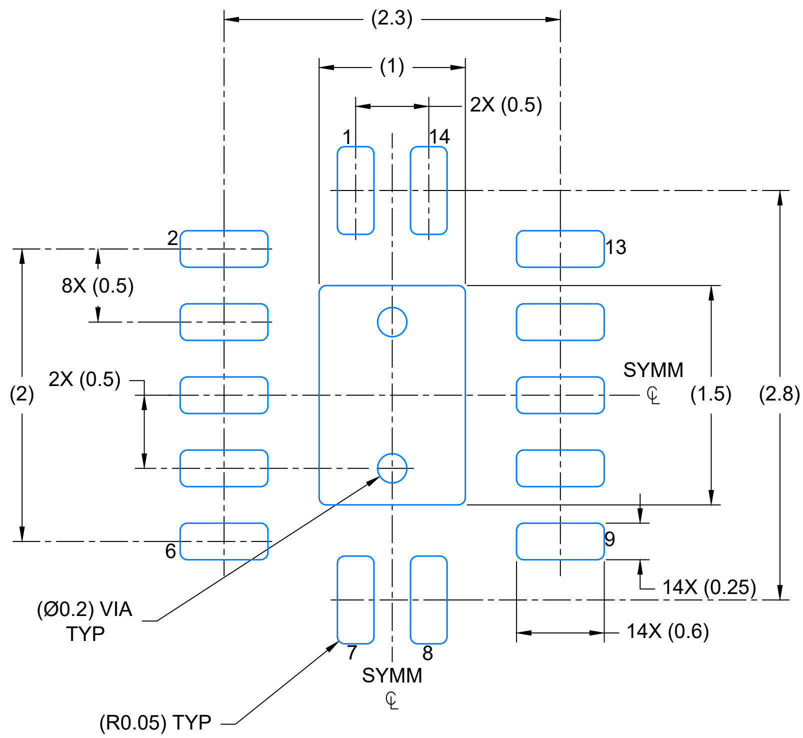
4227145/A



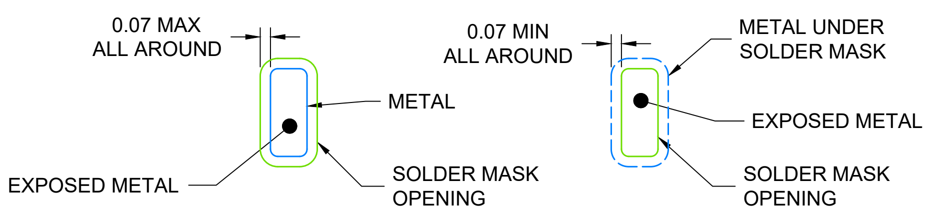
4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



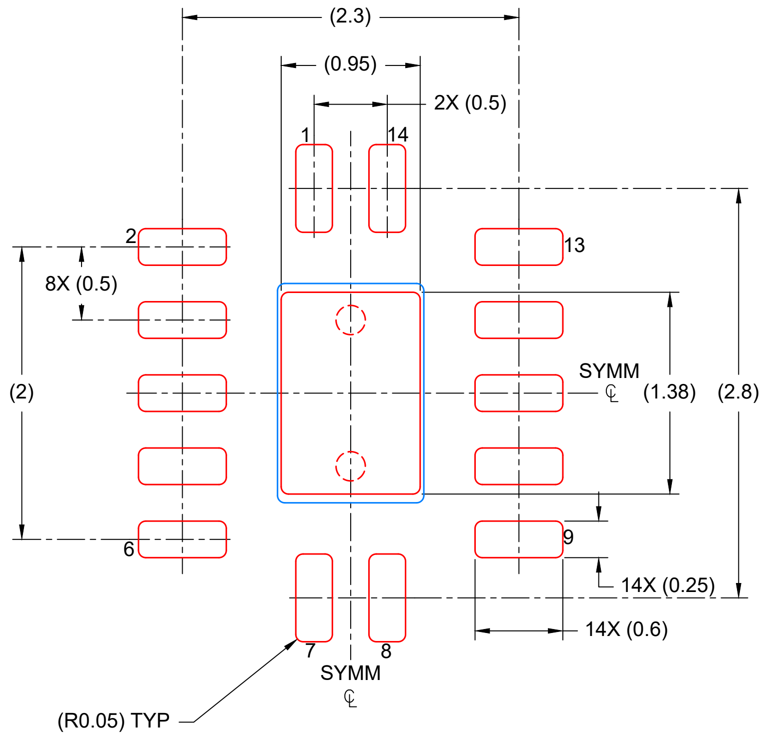
NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

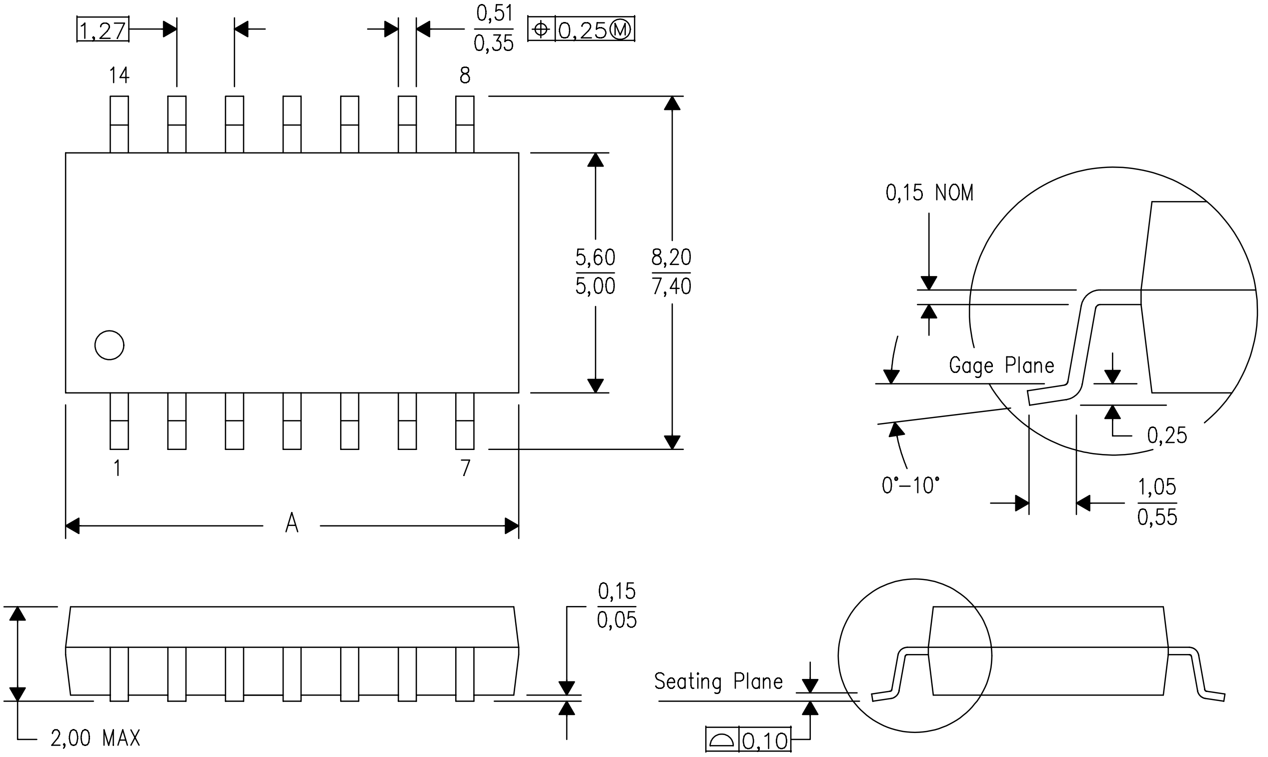
4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

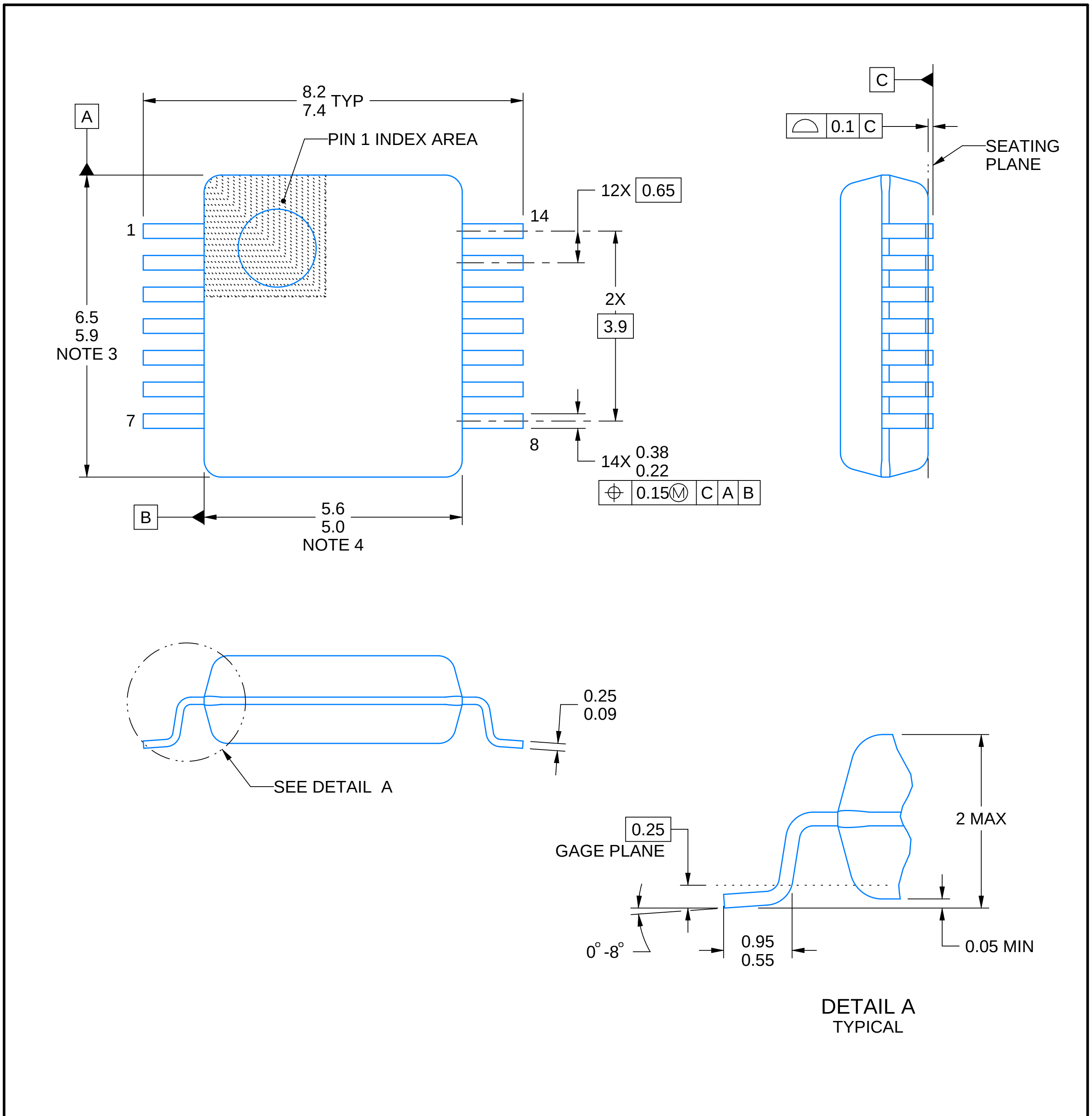
14-PINS SHOWN



PINS ** / DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



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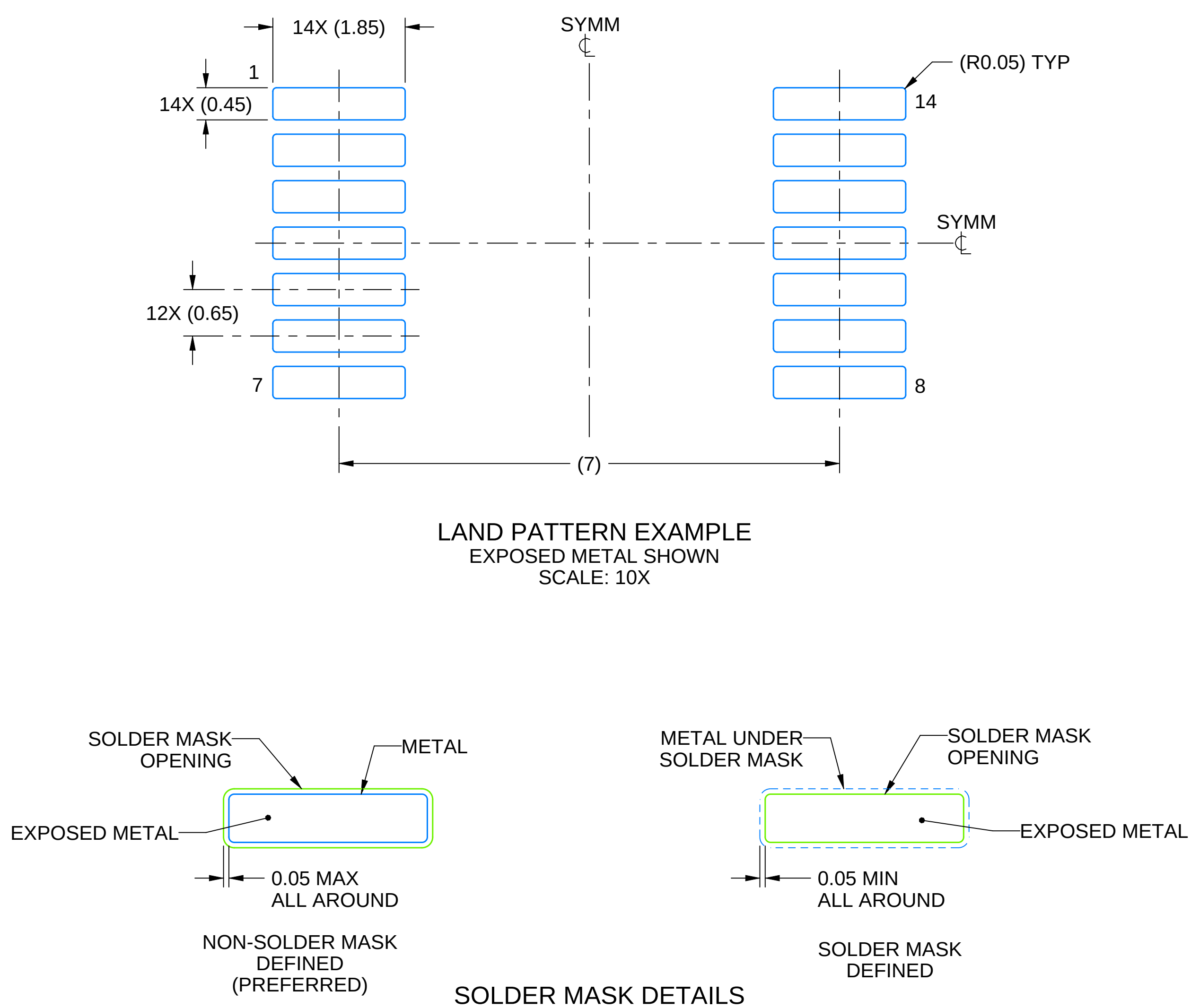
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



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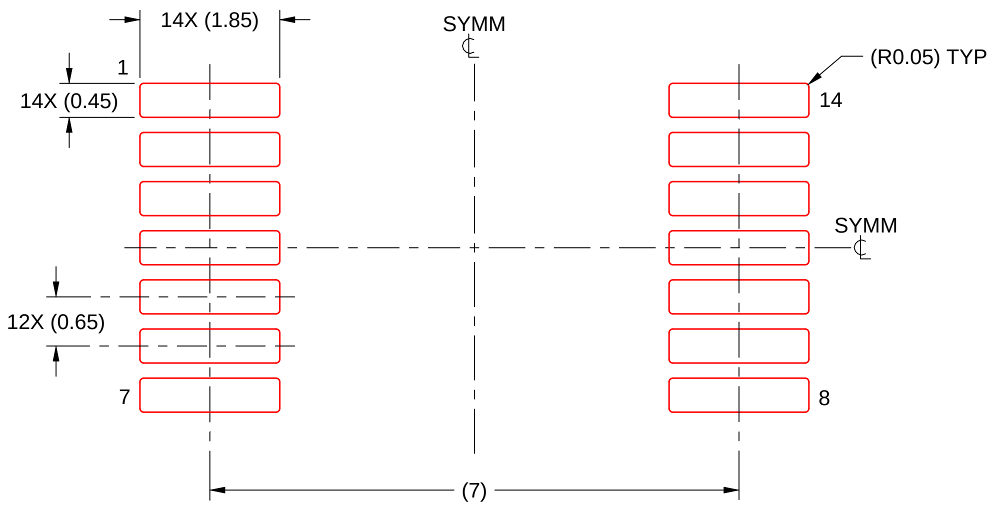
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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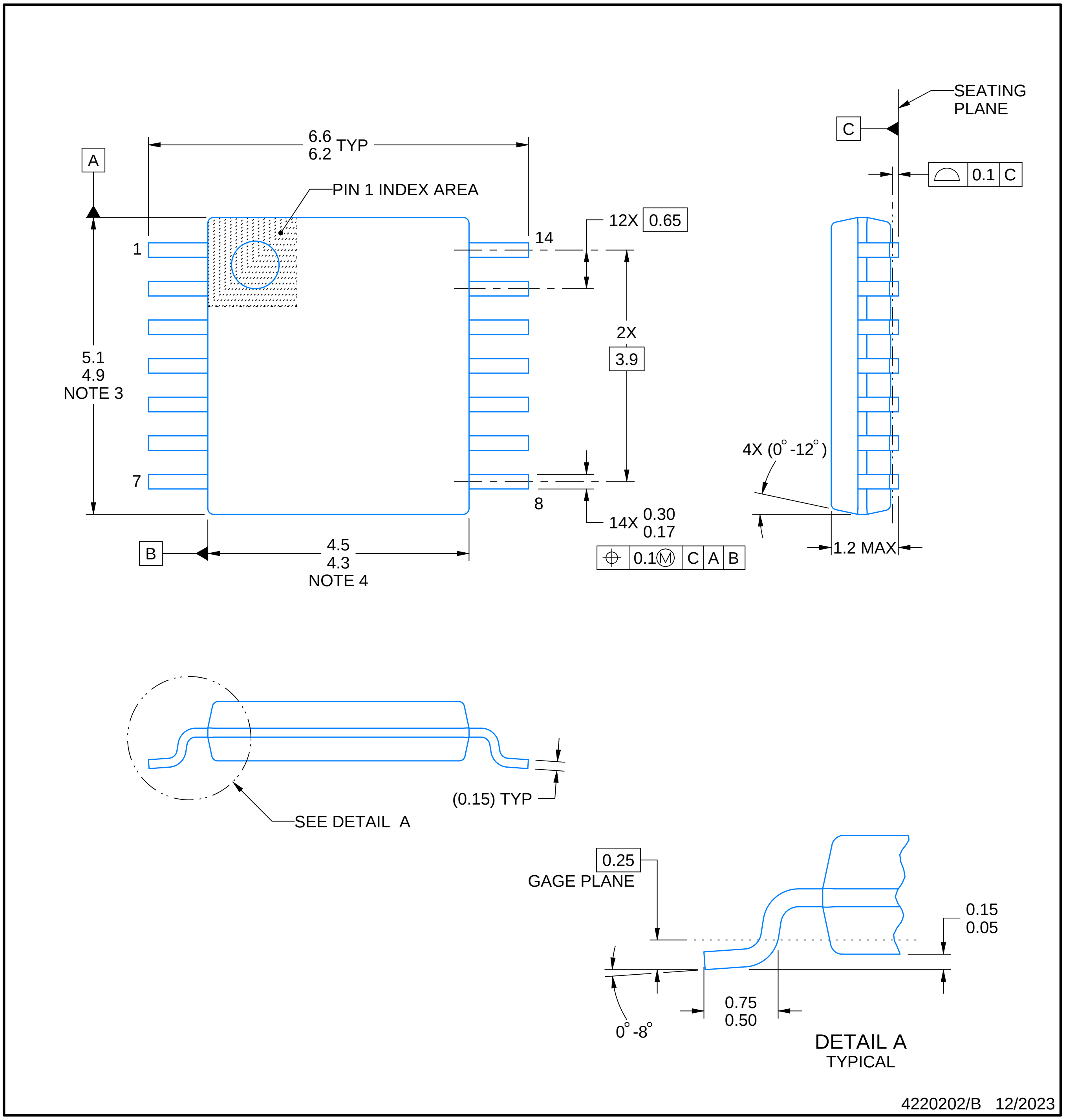
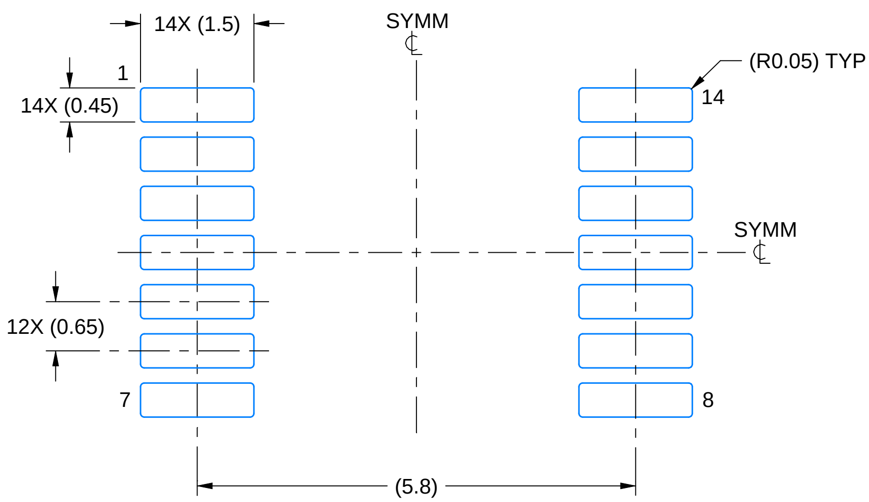
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

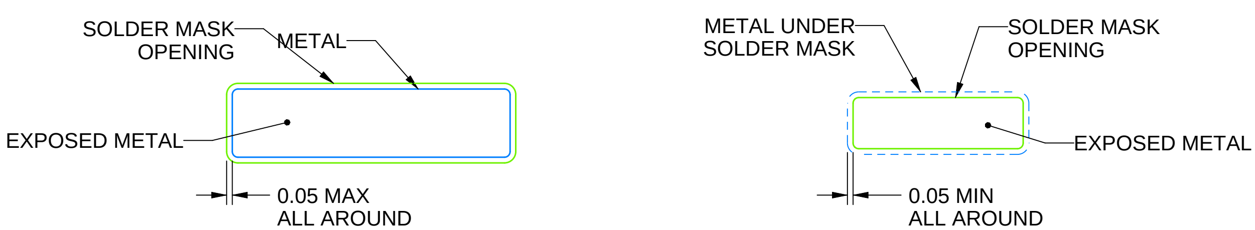


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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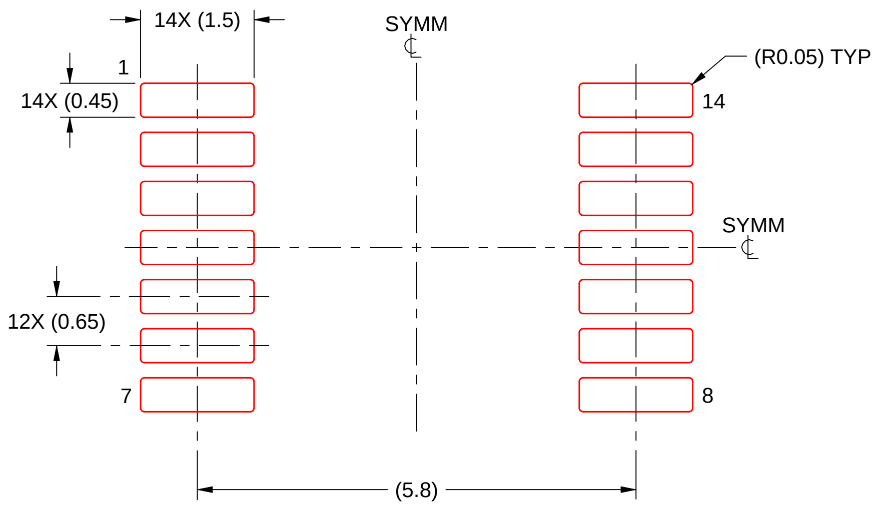
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.