# LOW-POWER DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

Check for Samples: SN74AUP2G80

FEATURES

- **Available in the Texas Instruments NanoStar™ Package**
- **Low Static-Power Consumption (I_{CC} = 0.9 µA Maximum)**
- **Low Dynamic-Power Consumption (C_{pd} = 4.3 pF Typ at 3.3 V)**
- **Low Input Capacitance (C_i = 1.5 pF Typical)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**

- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 4.4 ns Maximum at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
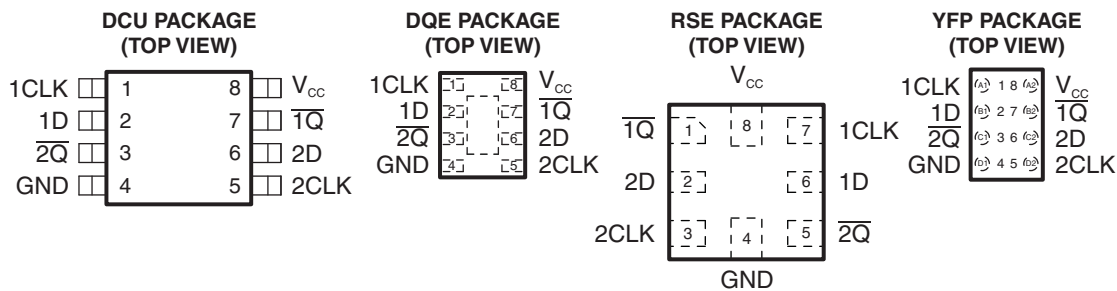
See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).
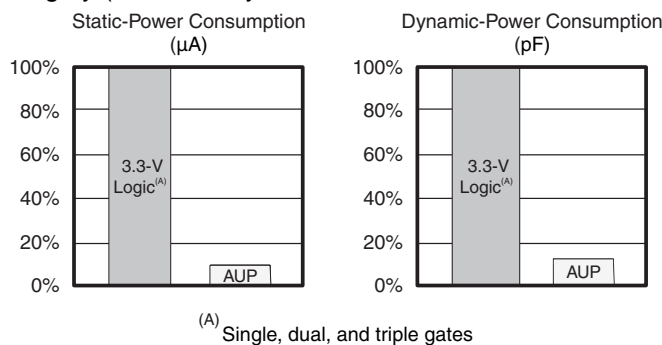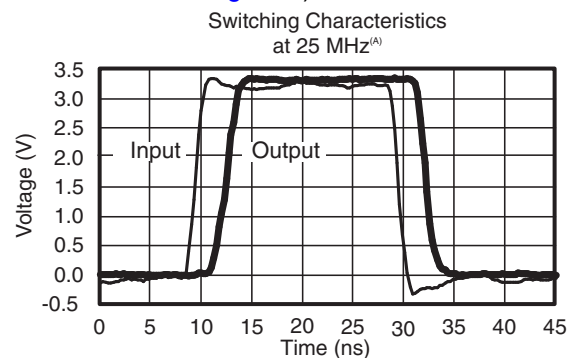

(A) Single, dual, and triple gates

Figure 1. AUP – The Lowest-Power Family

(A) SN74AUP2Gxx data at C_L = 15 pF.

Figure 2. Excellent Signal Integrity

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION[1]

T_A	PACKAGE[2]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[3]
−40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G80YFPR	_ _ _ H X _
	uQFN – DQE	Reel of 5000	SN74AUP2G80DQER	PU
	QFN – RSE	Reel of 5000	SN74AUP2G80RSER	PU
	SSOP – DCU	Reel of 3000	SN74AUP2G80DCUR	H80_

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	Q
↑	H	L
↑	L	H
L	X	Q_0

LOGIC DIAGRAM (POSITIVE LOGIC)
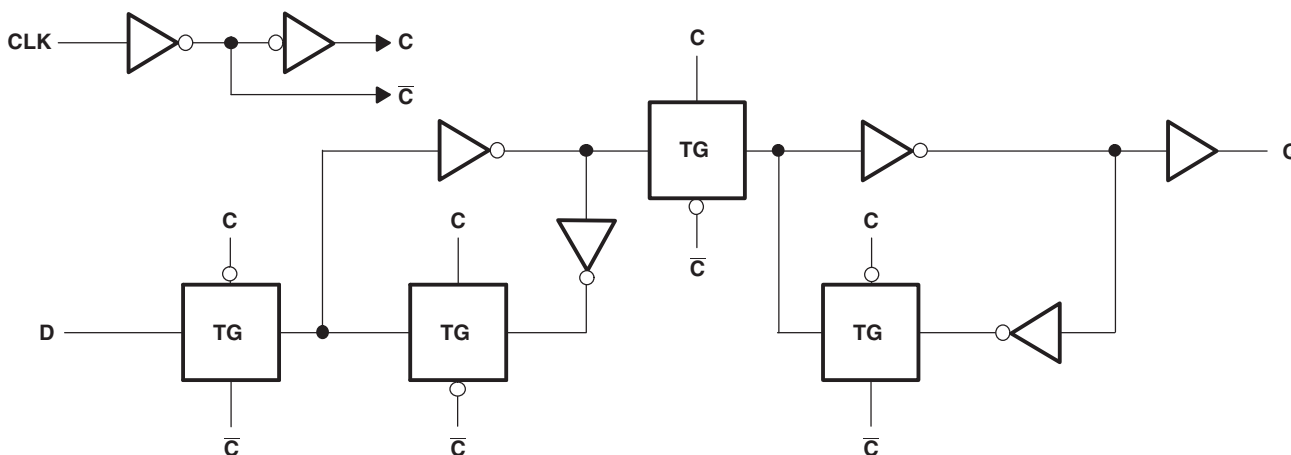
Pin numbers shown are for the DCU and DQE packages.

ABSOLUTE MAXIMUM RATINGS[(1)]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[(2)]		−0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[(2)]		−0.5	4.6	V
V_O	Output voltage range in the high or low state[(2)]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance[(3)]	DCU package		220	°C/W
		DQE package		261	
		RSE package		253	
		YFP package		132	
T_{stg}	Storage temperature range		−65	150	°C

(1)   Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3)   The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AUP2G80

RECOMMENDED OPERATING CONDITIONS[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	$0.65 \times V_{CC}$		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		$0.35 \times V_{CC}$	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		−20	µA
		V_{CC} = 1.1 V		−1.1	mA
		V_{CC} = 1.4 V		−1.7	
		V_{CC} = 1.65		−1.9	
		V_{CC} = 2.3 V		−3.1	
		V_{CC} = 3 V		−4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	µA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = −20 μA	0.8 V to 3.6 V	V_{CC} − 0.1			V_{CC} − 0.1		V
		I_{OH} = −1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
		I_{OH} = −1.7 mA	1.4 V	1.11			1.03		
		I_{OH} = −1.9 mA	1.65 V	1.32			1.3		
		I_{OH} = −2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = −3.1 mA		1.9			1.85		
		I_{OH} = −2.7 mA	3 V	2.72			2.67		
		I_{OH} = −4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 μA	0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	A or B input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	μA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	μA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	μA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), I_O = 0	0.8 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}		V_I = V_{CC} − 0.6 V[1], I_O = 0	3.3 V			40		50	μA
C_i		V_I = V_{CC} or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		V_O = GND	0 V		3				pF

(1)   One input at V_{CC} − 0.6 V, other input at V_{CC} or GND

Product Folder Link(s): SN74AUP2G80

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

		V_{CC}	T_A = 25°C	T_A = −40°C to 85°C		UNIT
			TYP	MIN	MAX	
f_{clock}	Clock frequency	0.8 V			20	MHz
		1.2 V ± 0.1 V			80	
		1.5 V ± 0.1 V			120	
		1.8 V ± 0.15 V			160	
		2.5 V ± 0.2 V			220	
		3.3 V ± 0.3 V			260	
t_w	Pulse duration, CLK high or low	0.8 V		5.5		
		1.2 V ± 0.1 V		2.5		
		1.5 V ± 0.1 V		1.5		
		1.8 V ± 0.15 V		1.6		
		2.5 V ± 0.2 V		1.7		
		3.3 V ± 0.3 V		1.9		
t_{su}	Setup time before CLK↑	Data high	0.8 V	3.4	6.7		ns
			1.2 V ± 0.1 V		2.4		
			1.5 V ± 0.1 V		1.2		
			1.8 V ± 0.15 V		0.8		
			2.5 V ± 0.2 V		0.6		
			3.3 V ± 0.3 V		0.4		
		Data low	0.8 V	3.4	8.9		ns
			1.2 V ± 0.1 V		2		
			1.5 V ± 0.1 V		1.3		
			1.8 V ± 0.15 V		1.1		
			2.5 V ± 0.2 V		0.8		
			3.3 V ± 0.3 V		0.7		
t_h	Hold time, data after CLK↑	0.8 V	0	1		ns
		1.2 V ± 0.1 V		0		
		1.5 V ± 0.1 V		0		
		1.8 V ± 0.15 V		0		
		2.5 V ± 0.2 V		0		
		3.3 V ± 0.3 V		0		

Product Folder Link(s): *SN74AUP2G80*

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		91		90		MHz
			1.2 V ± 0.1 V		175		220		
			1.5 V ± 0.1 V		237		230		
			1.8 V ± 0.15 V		269		240		
			2.5 V ± 0.2 V		280		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		17.2				ns
			1.2 V ± 0.1 V	3.2	7.1	14.9	2.7	16.3	
			1.5 V ± 0.1 V	1.9	5	9.8	2.1	10.3	
			1.8 V ± 0.15 V	1.7	3.9	7.6	1.6	8.1	
			2.5 V ± 0.2 V	1.4	2.8	5.3	1.2	5.6	
			3.3 V ± 0.3 V	1.2	2.2	4.1	1	4.4	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		68		70		MHz
			1.2 V ± 0.1 V		128		170		
			1.5 V ± 0.1 V		189		220		
			1.8 V ± 0.15 V		234		240		
			2.5 V ± 0.2 V		273		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		19.4				ns
			1.2 V ± 0.1 V	4.4	8.2	16.2	3.4	17.7	
			1.5 V ± 0.1 V	3.6	5.8	10.7	2.6	11.3	
			1.8 V ± 0.15 V	2.9	4.6	8.4	2.1	3	
			2.5 V ± 0.2 V	2.2	3.3	5.9	1.7	6.3	
			3.3 V ± 0.3 V	1.9	2.7	4.7	1.4	4.9	

SN74AUP2G80

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		52		50		MHz
			1.2 V ± 0.1 V		98		130		
			1.5 V ± 0.1 V		148		180		
			1.8 V ± 0.15 V		196		240		
			2.5 V ± 0.2 V		249		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		21.5				ns
			1.2 V ± 0.1 V	3	9.1	17.4	4.1	19	
			1.5 V ± 0.1 V	3.2	6.5	11.7	3.2	12.3	
			1.8 V ± 0.15 V	2.7	4.2	9.2	2.6	9.8	
			2.5 V ± 0.2 V	2.2	3.8	6.5	2.1	6.9	
			3.3 V ± 0.3 V	1.9	3.1	5.1	1.8	5.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = −40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		32		20		MHz
			1.2 V ± 0.1 V		71		80		
			1.5 V ± 0.1 V		104		120		
			1.8 V ± 0.15 V		133		160		
			2.5 V ± 0.2 V		181		220		
			3.3 V ± 0.3 V		257		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		28.4				ns
			1.2 V ± 0.1 V	5.1	11.8	20.7	6.2	28.7	
			1.5 V ± 0.1 V	4.8	8.5	14.1	6.9	16.7	
			1.8 V ± 0.15 V	4	6.9	11.2	2	13.3	
			2.5 V ± 0.2 V	3.3	5.1	7.9	3.2	9.3	
			3.3 V ± 0.3 V	2.9	4.2	6.4	2.8	7.5	

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

Product Folder Link(s): *SN74AUP2G80*

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)

From Output
Under Test

C_L
(see Note A)   1 MΩ
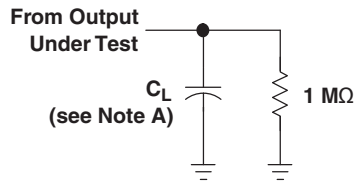
LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	V_{CC}/2	V_{CC}/2	V_{CC}/2	V_{CC}/2	V_{CC}/2	V_{CC}/2
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, for propagation delays t_r/t_f = 3 ns, for setup and hold times and pulse width t_r/t_f = 1.2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.
F. All parameters and waveforms are not applicable to all devices.
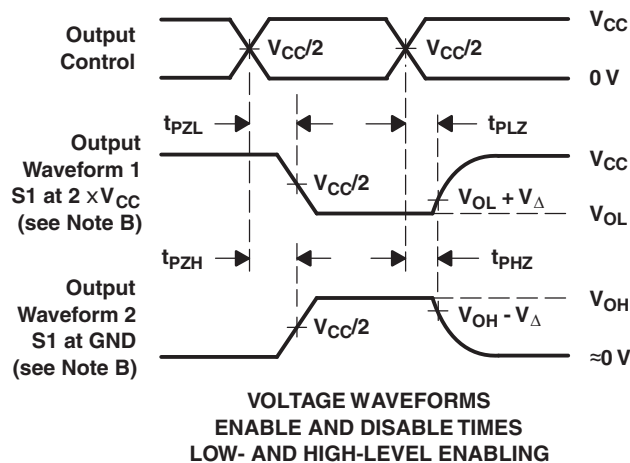
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)

From Output Under Test — 5 kΩ — S1 — $2 \times V_{CC}$ / GND

C_L (see Note A) 5 kΩ
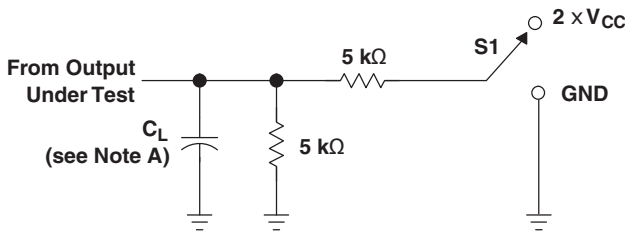
LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V

Output Control

Output Waveform 1 S1 at $2 \times V_{CC}$ (see Note B) — t_{PZL}, t_{PLZ}

Output Waveform 2 S1 at GND (see Note B) — t_{PZH}, t_{PHZ}

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PLH} and t_{PHL} are the same as t_{pd}.

G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

Product Folder Link(s): SN74AUP2G80

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP2G80DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H80R	Samples
SN74AUP2G80DQER	ACTIVE	X2SON	DQE	8	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PU	Samples
SN74AUP2G80RSER	ACTIVE	UQFN	RSE	8	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	PU	Samples
SN74AUP2G80YFPR	NRND	DSBGA	YFP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HXN	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G80DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUP2G80DQER	X2SON	DQE	8	5000	180.0	8.4	1.2	1.6	0.55	4.0	8.0	Q1
SN74AUP2G80RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
SN74AUP2G80YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G80DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUP2G80DQER	X2SON	DQE	8	5000	202.0	201.0	28.0
SN74AUP2G80RSER	UQFN	RSE	8	5000	202.0	201.0	28.0
SN74AUP2G80YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0

3.2
3.0 TYP

A

PIN 1 INDEX AREA

1

2.1
1.9
NOTE 3

4

8

6X 0.5

2X

1.5

5

8X 0.25
0.17

⊕ 0.08Ⓜ C A B

B

2.4
2.2
NOTE 3

C

⌒ 0.1 C

SEATING
PLANE

SEE DETAIL A

(0.13) TYP

0.12
GAGE PLANE

0°-6°

0.35
0.20

0.9
0.6

0.1
0.0

DETAIL A
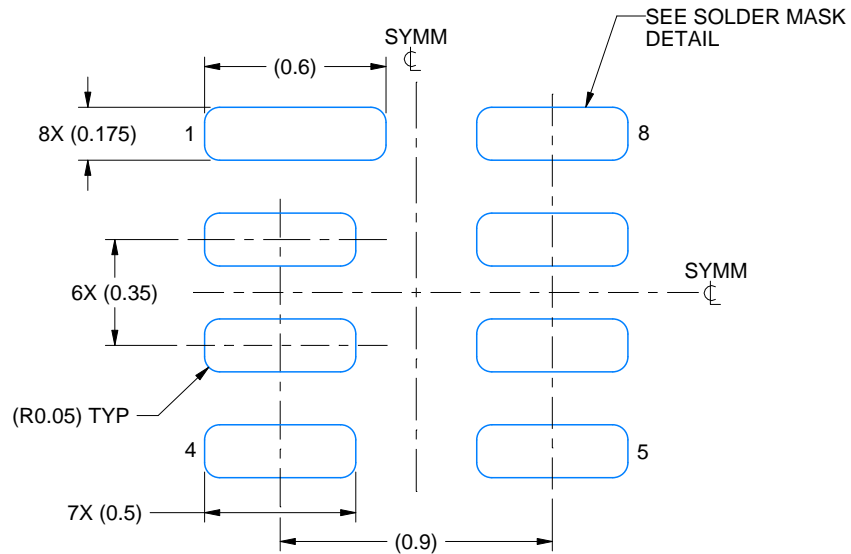TYPICAL
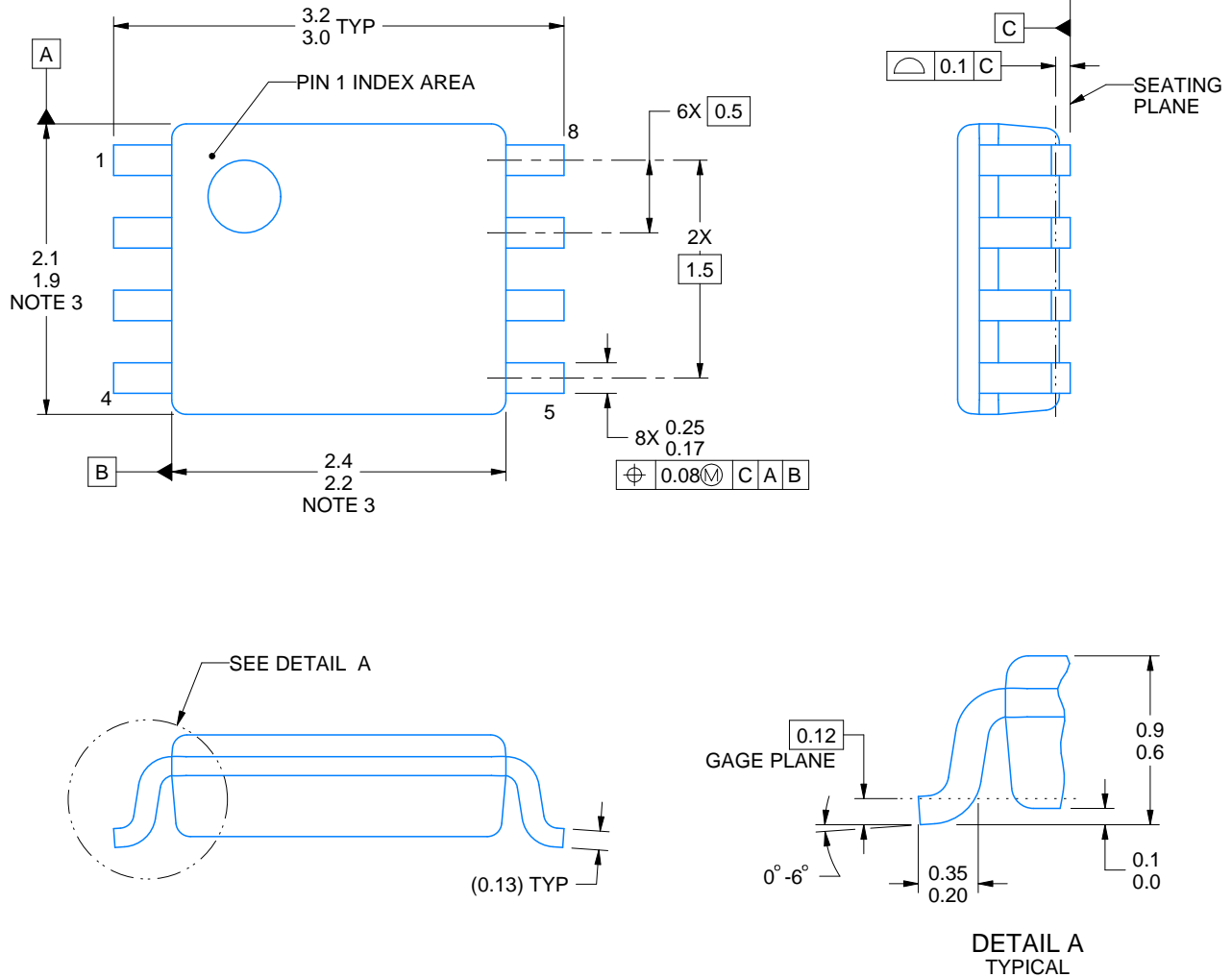
4225266/A   09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

SEE SOLDER MASK
DETAILS

8X (0.85)

SYMM

(R0.05) TYP

8X (0.3)   1   8

                                                           SYMM

6X (0.5)

4   5

(3.1)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

SOLDER MASK
OPENING   METAL   METAL UNDER   SOLDER MASK
                                          SOLDER MASK   OPENING

EXPOSED METAL   EXPOSED METAL

            0.05 MAX   0.05 MIN
            ALL AROUND   ALL AROUND

NON-SOLDER MASK   SOLDER MASK
DEFINED   DEFINED
(PREFERRED)
                        SOLDER MASK DETAILS
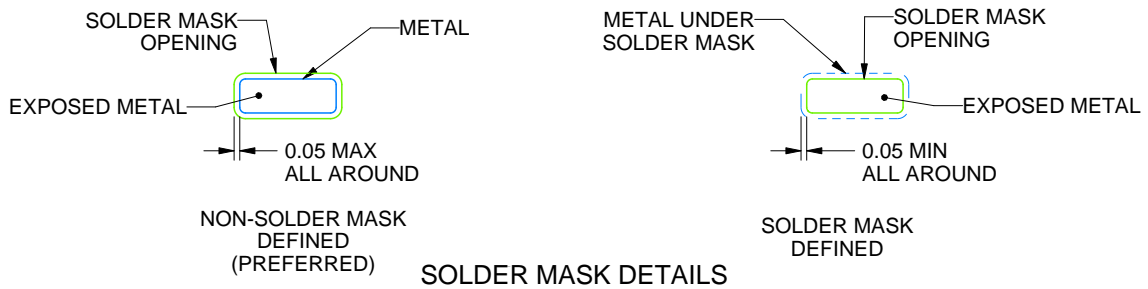
4225266/A   09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DCU0008A

8X (0.85)

SYMM

(R0.05) TYP

8X (0.3)   1
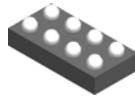
8

6X (0.5)

SYMM

4

5

(3.1)
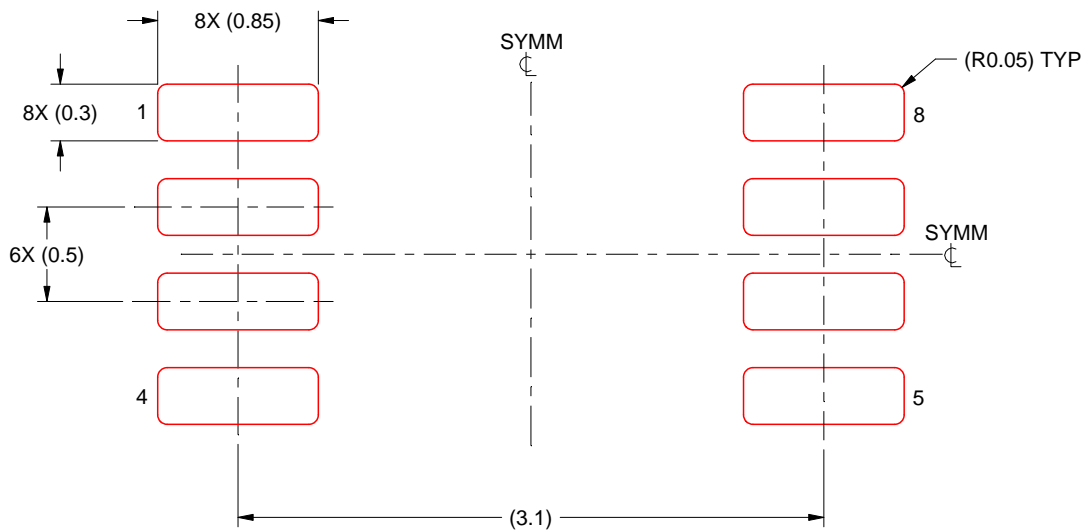
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A   09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
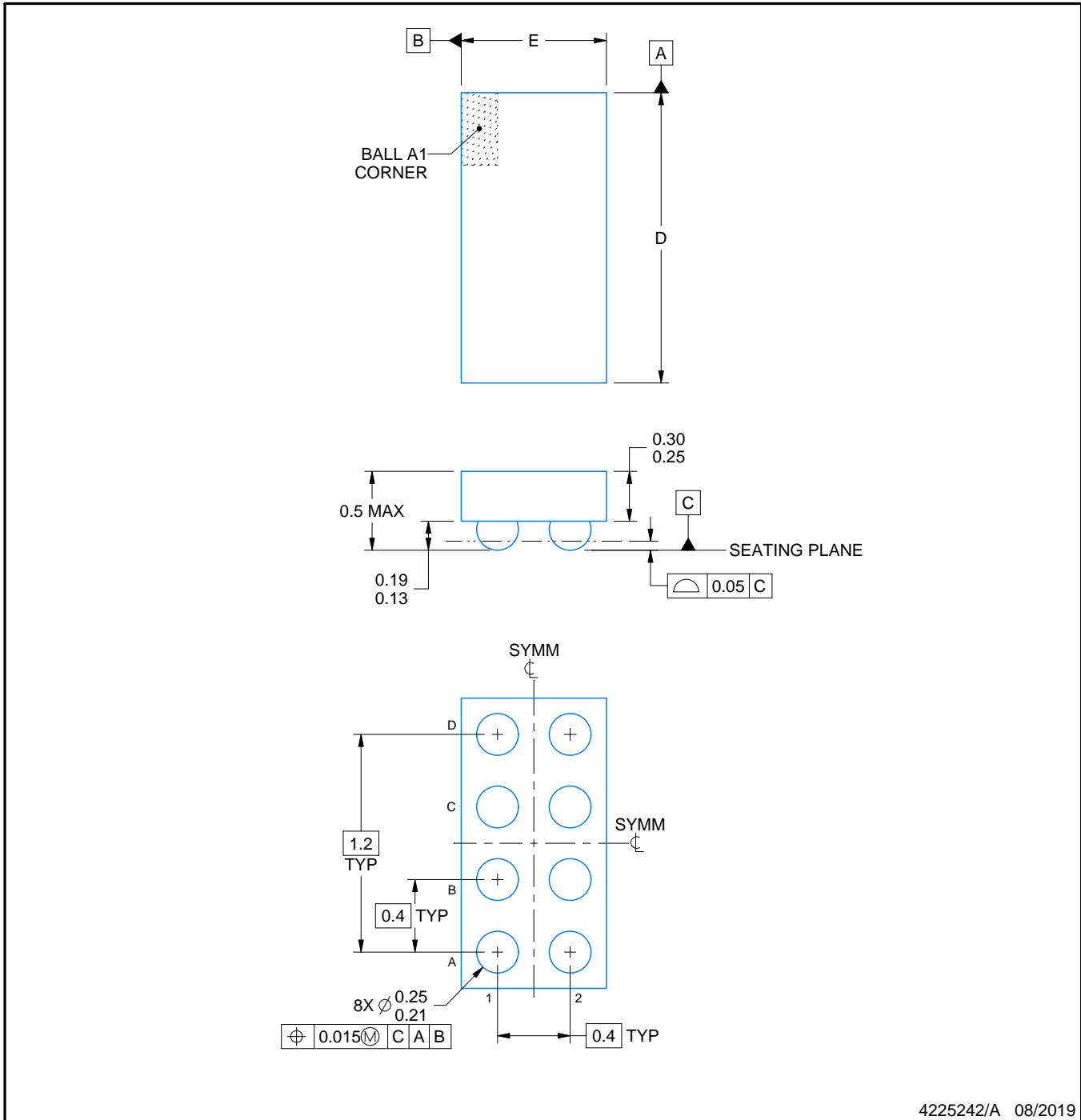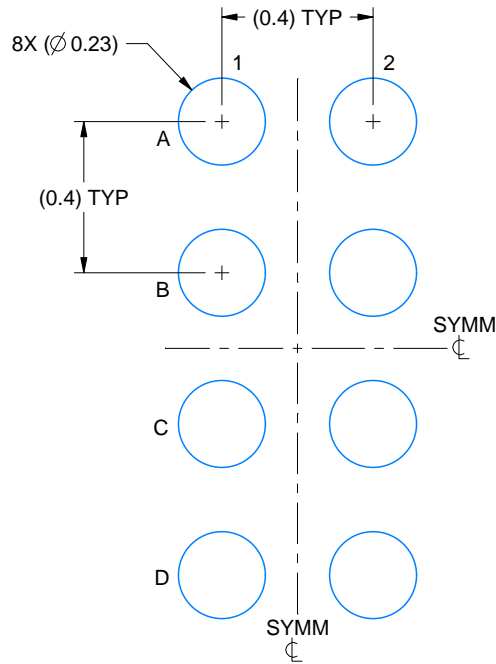8. Board assembly site may have different recommendations for stencil design.
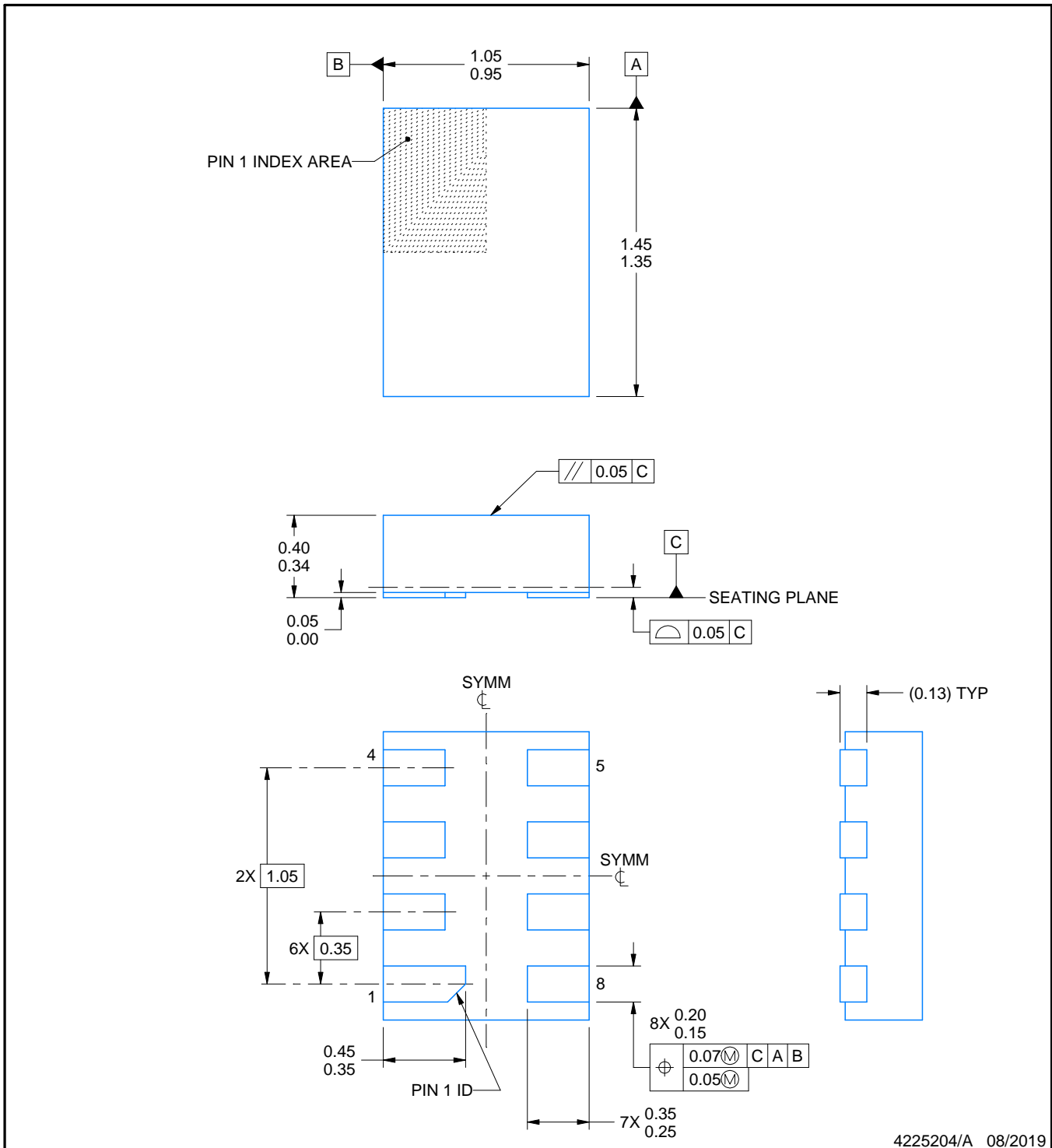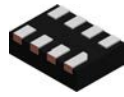
B | 1.05 / 0.95 | A

PIN 1 INDEX AREA

1.45 / 1.35

// 0.05 C

0.40 / 0.34

0.05 / 0.00

C

SEATING PLANE

0.05 C

SYMM

4

5

2X 1.05

SYMM

6X 0.35

1

8

0.45 / 0.35

PIN 1 ID

8X 0.20 / 0.15

⊕ 0.07 M C A B

0.05 M

7X 0.35 / 0.25

(0.13) TYP

4225204/A   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
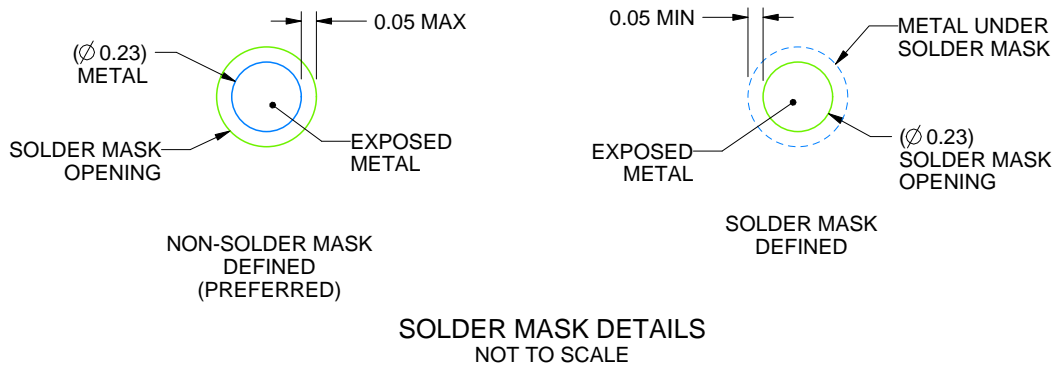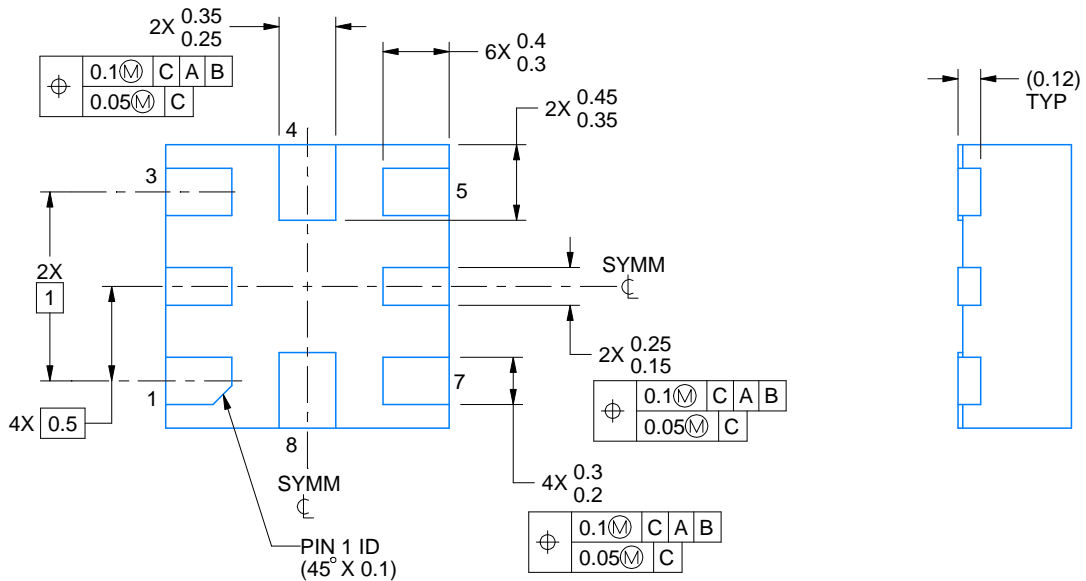2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-287 variation X2EAF.

DQE0008A

SEE SOLDER MASK
DETAIL

SYMM

(0.6)

8X (0.175)   1   8

6X (0.35)

SYMM

(R0.05) TYP

4   5

7X (0.5)

(0.9)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

0.05 MAX
ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED
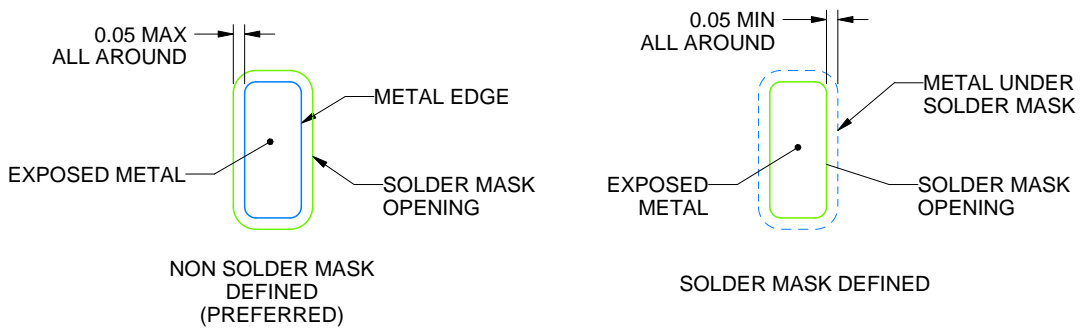
SOLDER MASK DETAILS

4225204/A   08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).

TEXAS INSTRUMENTS
www.ti.com

DQE0008A

8X (0.175)

(0.6)

6X (0.35)

(R0.05) TYP
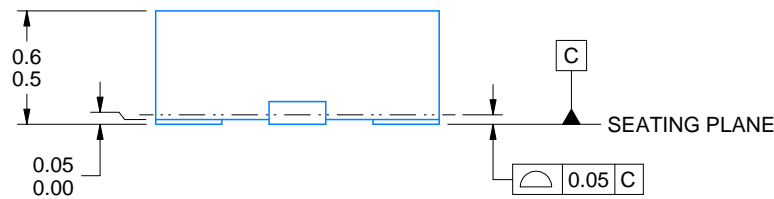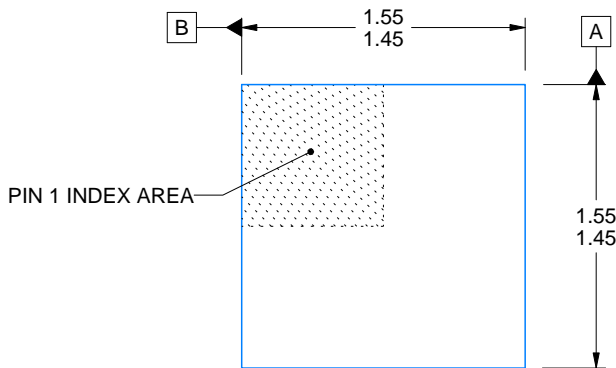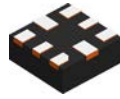
7X (0.5)

(0.9)

SYMM

SYMM
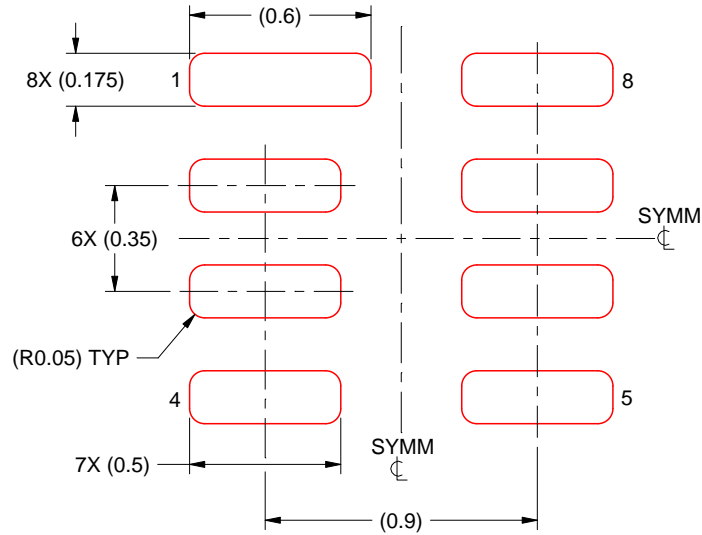
SOLDER PASTE EXAMPLE
BASED ON 0.075 MM THICK STENCIL
SCALE: 40X

4225204/A   08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

B ← E → A

BALL A1
CORNER

D

0.30
0.25

0.5 MAX

C

SEATING PLANE

0.19
0.13

⬡ 0.05 C

SYMM

1.2
TYP

D

C

SYMM

B

0.4 TYP

A

8X ⌀ 0.25
0.21

1   2

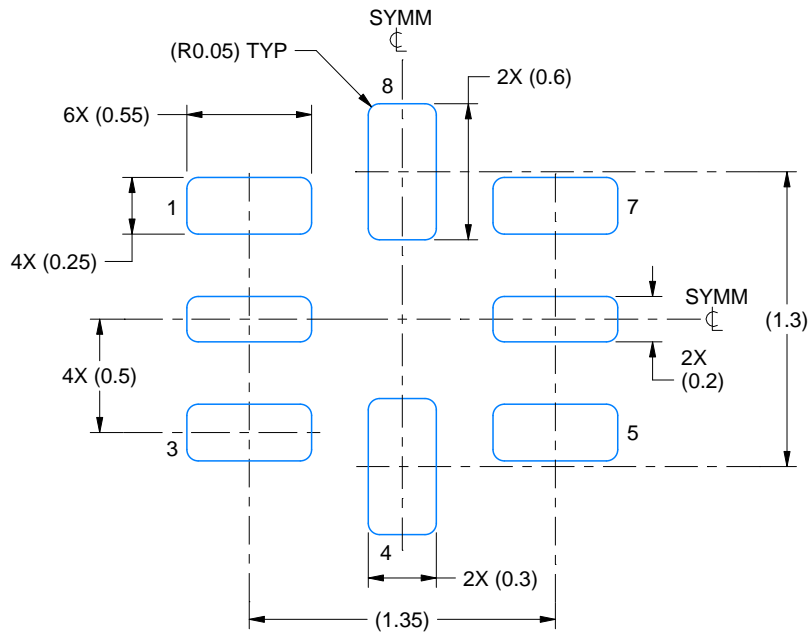⊕ 0.015Ⓜ C A B

0.4 TYP

4225242/A   08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
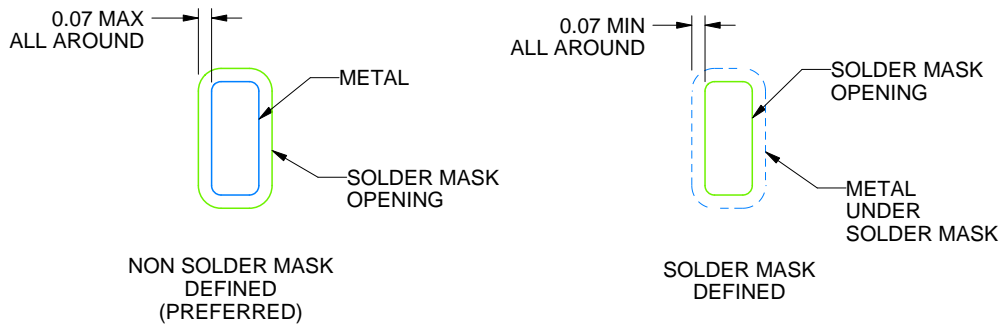2. This drawing is subject to change without notice.

8X (⌀ 0.23)

(0.4) TYP

(0.4) TYP

1

2

A

B

SYMM
₵

C

D

SYMM
₵

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

0.05 MAX

(⌀ 0.23)
METAL

SOLDER MASK
OPENING

EXPOSED
METAL

**NON-SOLDER MASK
DEFINED
(PREFERRED)**

0.05 MIN

METAL UNDER
SOLDER MASK

EXPOSED
METAL

(⌀ 0.23)
SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS
NOT TO SCALE

4225242/A   08/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

YFP0008

8X (□ 0.25)

(0.4) TYP

(R0.05) TYP

(0.4) TYP

METAL TYP

SYMM ℄

SYMM ℄
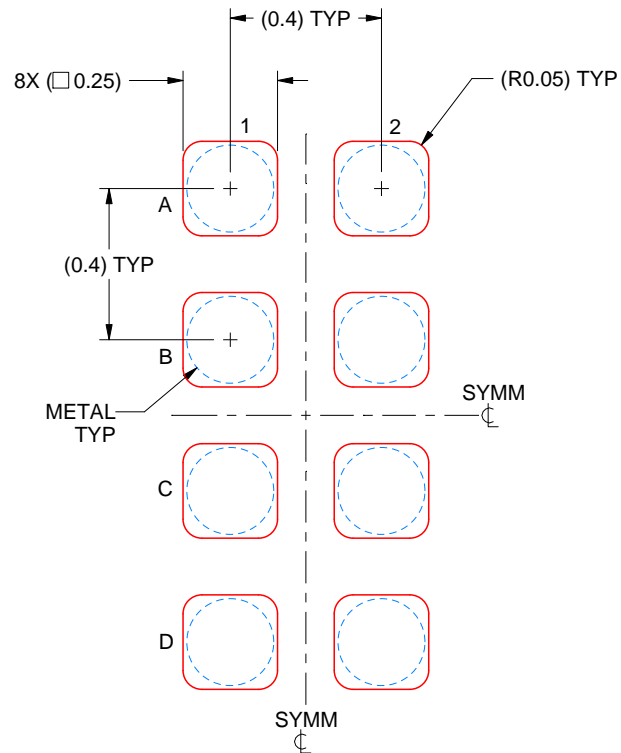
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4225242/A   08/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

B

1.55
1.45

A

PIN 1 INDEX AREA

1.55
1.45

0.6
0.5

C

SEATING PLANE

0.05
0.00

⌒ | 0.05 | C

2X 0.35
0.25

⊕ | 0.1 Ⓜ | C | A | B
| 0.05 Ⓜ | C

6X 0.4
0.3

2X 0.45
0.35

4

3

5

2X
| 1 |

SYMM
₵

2X 0.25
0.15

1

⊕ | 0.1 Ⓜ | C | A | B
| 0.05 Ⓜ | C

4X | 0.5 |

8

7

SYMM
₵

4X 0.3
0.2

⊕ | 0.1 Ⓜ | C | A | B
| 0.05 Ⓜ | C

PIN 1 ID
(45° X 0.1)

(0.12)
TYP

4220323/B   03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

TEXAS INSTRUMENTS

www.ti.com

SYMM

(R0.05) TYP

2X (0.6)

6X (0.55)

4X (0.25)

SYMM

(1.3)

4X (0.5)

2X (0.2)

2X (0.3)

(1.35)

LAND PATTERN EXAMPLE
SCALE:30X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

**NON SOLDER MASK
DEFINED
(PREFERRED)**

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL
UNDER
SOLDER MASK

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS
NOT TO SCALE

4220323/B   03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/B   03/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

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