

## SN74ALVCH16245 16-Bit Bus Transceiver With 3-State Outputs

### 1 Features

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 3 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

### 2 Applications

- Cable Modem Termination Systems
- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

### 3 Description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16245 device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic high or low level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

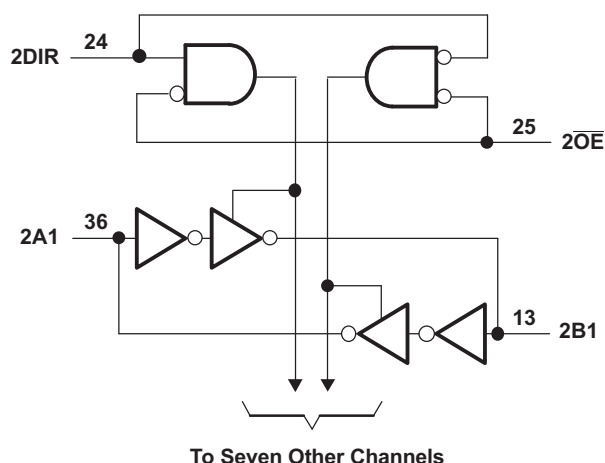
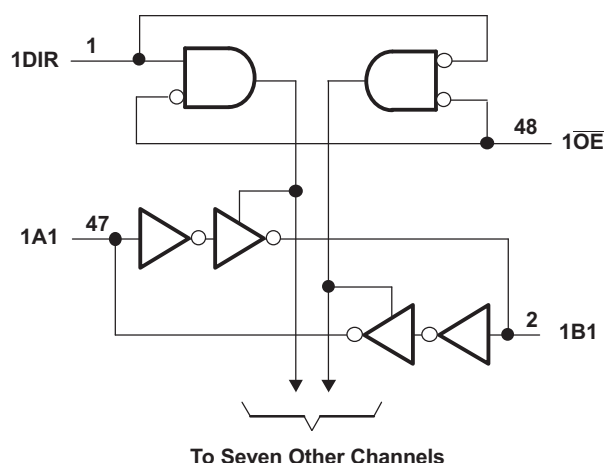
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

#### Device Information<sup>(1)</sup>

| PART NUMBER       | PACKAGE                   | BODY SIZE (NOM)    |
|-------------------|---------------------------|--------------------|
| SN74ALVCH16245ZRD | BGA MICROSTAR JUNIOR (56) | 4.50 mm × 7.00 mm  |
| SN74ALVCH16245ZQL | BGA MICROSTAR JUNIOR (54) | 5.50 mm × 8.00 mm  |
| SN74ALVCH16245DGG | TSSOP (48)                | 6.10 mm × 12.50 mm |
| SN74ALVCH16245DGV | TVSOP (48)                | 4.40 mm × 9.70 mm  |
| SN74ALVCH16245DL  | SSOP (48)                 | 7.50 mm × 15.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



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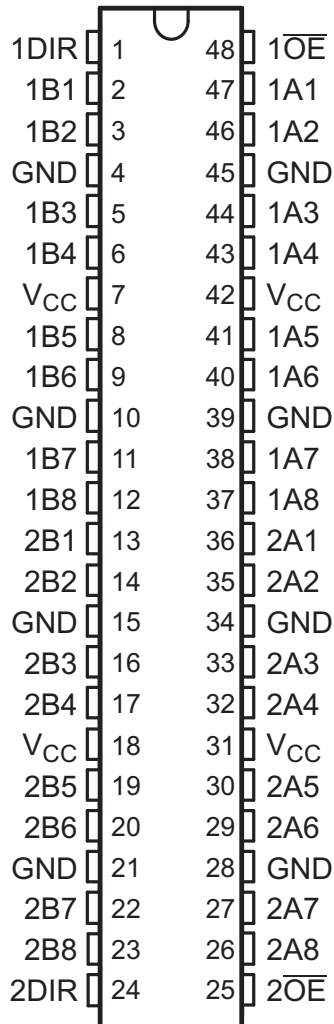
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

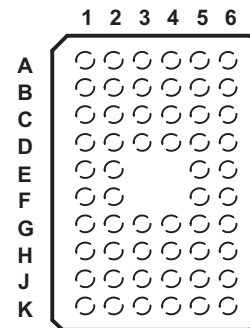
| Changes from Revision L (November 2005) to Revision M                                                                                                                                                                                                                                                                                      | Page     |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| <ul style="list-style-type: none"> <li>Added ESD Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ....</li> </ul> | <b>1</b> |

## 5 Pin Configuration and Functions

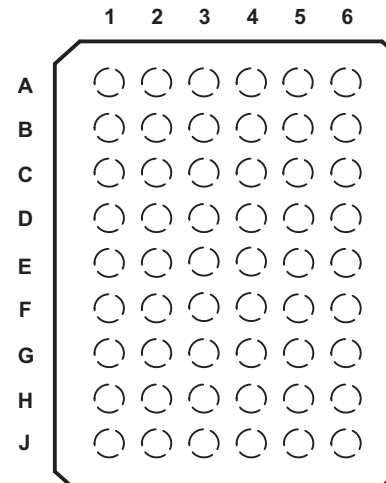
**DGG, DGV, or DL Package  
48-Pin TSSOP, TVSOP, or SSOP  
Top View**



**GQL or ZQL Package  
56-Pin BGA MICROSTAR JUNIOR  
Top View**



**GRD or ZRD Package  
54-Pin BGA MICROSTAR JUNIOR  
Top View**



### Pin Functions

| NAME | PIN                      |           |           | I/O | DESCRIPTION         |
|------|--------------------------|-----------|-----------|-----|---------------------|
|      | TSSOP,<br>TVSOP,<br>SSOP | FBGA (56) | FBGA (54) |     |                     |
| 1A1  | 47                       | B5        | A6        | I/O | Transceiver I/O pin |
| 1A2  | 46                       | B6        | B5        | I/O | Transceiver I/O pin |
| 1A3  | 44                       | C5        | B6        | I/O | Transceiver I/O pin |
| 1A4  | 43                       | C6        | C5        | I/O | Transceiver I/O pin |
| 1A5  | 41                       | D5        | C6        | I/O | Transceiver I/O pin |
| 1A6  | 40                       | D6        | D5        | I/O | Transceiver I/O pin |
| 1A7  | 38                       | E5        | D6        | I/O | Transceiver I/O pin |
| 1A8  | 37                       | E6        | E5        | I/O | Transceiver I/O pin |
| 2A1  | 36                       | F6        | E6        | I/O | Transceiver I/O pin |
| 2A2  | 35                       | F5        | F5        | I/O | Transceiver I/O pin |
| 2A3  | 33                       | G6        | F6        | I/O | Transceiver I/O pin |

### Pin Functions (continued)

| NAME             | PIN                      |                                |                                | I/O | DESCRIPTION                                                                                                   |
|------------------|--------------------------|--------------------------------|--------------------------------|-----|---------------------------------------------------------------------------------------------------------------|
|                  | TSSOP,<br>TVSOP,<br>SSOP | FBGA (56)                      | FBGA (54)                      |     |                                                                                                               |
| 2A4              | 32                       | G5                             | G5                             | I/O | Transceiver I/O pin                                                                                           |
| 2A5              | 30                       | H6                             | G6                             | I/O | Transceiver I/O pin                                                                                           |
| 2A6              | 29                       | H5                             | H5                             | I/O | Transceiver I/O pin                                                                                           |
| 2A7              | 27                       | J6                             | H6                             | I/O | Transceiver I/O pin                                                                                           |
| 2A8              | 26                       | J5                             | J6                             | I/O | Transceiver I/O pin                                                                                           |
| 1DIR             | 1                        | A1                             | A3                             | I   | Direction control. When high, the signal propagates from A to B. When low, the signal propagates from B to A. |
| $\overline{1OE}$ | 48                       | A6                             | A4                             | I   | Output enable                                                                                                 |
| 2DIR             | 24                       | K1                             | J3                             | I   | Direction control. When high, the signal propagates from A to B. When low, the signal propagates from B to A. |
| $\overline{2OE}$ | 25                       | K6                             | J4                             | I   | Output enable                                                                                                 |
| 1B1              | 2                        | B2                             | A1                             | I/O | Transceiver I/O pin                                                                                           |
| 1B2              | 3                        | B1                             | B2                             | I/O | Transceiver I/O pin                                                                                           |
| 1B3              | 5                        | C2                             | B1                             | I/O | Transceiver I/O pin                                                                                           |
| 1B4              | 6                        | C1                             | C2                             | I/O | Transceiver I/O pin                                                                                           |
| 1B5              | 8                        | D2                             | C1                             | I/O | Transceiver I/O pin                                                                                           |
| 1B6              | 9                        | D1                             | D2                             | I/O | Transceiver I/O pin                                                                                           |
| 1B7              | 11                       | E2                             | D1                             | I/O | Transceiver I/O pin                                                                                           |
| 1B8              | 12                       | E1                             | E2                             | I/O | Transceiver I/O pin                                                                                           |
| 2B1              | 13                       | F1                             | E1                             | I/O | Transceiver I/O pin                                                                                           |
| 2B2              | 14                       | F2                             | F2                             | I/O | Transceiver I/O pin                                                                                           |
| 2B3              | 16                       | G1                             | F1                             | I/O | Transceiver I/O pin                                                                                           |
| B4               | 17                       | G2                             | G2                             | I/O | Transceiver I/O pin                                                                                           |
| 2B5              | 19                       | H1                             | G1                             | I/O | Transceiver I/O pin                                                                                           |
| 2B6              | 20                       | H2                             | H2                             | I/O | Transceiver I/O pin                                                                                           |
| 2B7              | 22                       | J1                             | H1                             | I/O | Transceiver I/O pin                                                                                           |
| 2B8              | 23                       | J2                             | J1                             | I/O | Transceiver I/O pin                                                                                           |
| GND              | 4,10,15,21,28,34,39,45   | B3, B4, D3, D4, G3, G4, J3, J4 | D3, D4, E3, E4, F3, F4         | —   | Ground                                                                                                        |
| V <sub>CC</sub>  | 7,18,31,42               | C3, C4, H3, H4                 | C3, C4, G3, G4                 | —   | Power pin                                                                                                     |
| NC               | —                        | A2, A3, A4, A5, K2, K3, K4, K5 | A2, A5, B3, B4, H3, H4, J2, J5 | —   | No connect                                                                                                    |

### Pin Assignments<sup>(1)</sup> (56-Ball GQL or ZQL Package)

|          | 1    | 2   | 3               | 4               | 5   | 6                |
|----------|------|-----|-----------------|-----------------|-----|------------------|
| <b>A</b> | 1DIR | NC  | NC              | NC              | NC  | $\overline{1OE}$ |
| <b>B</b> | 1B2  | 1B1 | GND             | GND             | 1A1 | 1A2              |
| <b>C</b> | 1B4  | 1B3 | V <sub>CC</sub> | V <sub>CC</sub> | 1A3 | 1A4              |
| <b>D</b> | 1B6  | 1B5 | GND             | GND             | 1A5 | 1A6              |
| <b>E</b> | 1B8  | 1B7 |                 |                 | 1A7 | 1A8              |
| <b>F</b> | 2B1  | 2B2 |                 |                 | 2A2 | 2A1              |
| <b>G</b> | 2B3  | 2B4 | GND             | GND             | 2A4 | 2A3              |
| <b>H</b> | 2B5  | 2B6 | V <sub>CC</sub> | V <sub>CC</sub> | 2A6 | 2A5              |
| <b>J</b> | 2B7  | 2B8 | GND             | GND             | 2A8 | 2A7              |
| <b>K</b> | 2DIR | NC  | NC              | NC              | NC  | $\overline{2OE}$ |

(1) NC – No internal connection

**Pin Assignments <sup>(1)</sup>  
(54-Ball GRD or ZRD Package)**

|          | 1   | 2   | 3               | 4                | 5   | 6   |
|----------|-----|-----|-----------------|------------------|-----|-----|
| <b>A</b> | 1B1 | NC  | 1DIR            | $\overline{1OE}$ | NC  | 1A1 |
| <b>B</b> | 1B3 | 1B2 | NC              | NC               | 1A2 | 1A3 |
| <b>C</b> | 1B5 | 1B4 | V <sub>CC</sub> | V <sub>CC</sub>  | 1A4 | 1A5 |
| <b>D</b> | 1B7 | 1B6 | GND             | GND              | 1A6 | 1A7 |
| <b>E</b> | 2B1 | 1B8 | GND             | GND              | 1A8 | 2A1 |
| <b>F</b> | 2B3 | 2B2 | GND             | GND              | 2A2 | 2A3 |
| <b>G</b> | 2B5 | 2B4 | V <sub>CC</sub> | V <sub>CC</sub>  | 2A4 | 2A5 |
| <b>H</b> | 2B7 | 2B6 | NC              | NC               | 2A6 | 2A7 |
| <b>J</b> | 2B8 | NC  | 2DIR            | $\overline{2OE}$ | NC  | 2A8 |

(1) NC – No internal connection

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                        | MIN                | MAX                   | UNIT |
|------------------|--------------------------------------------------------|--------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage                                         | −0.5               | 4.6                   | V    |
| V <sub>I</sub>   | Input voltage <sup>(2)(3)</sup>                        | −0.5               | V <sub>CC</sub> + 0.5 | V    |
| V <sub>O</sub>   | Output voltage <sup>(2)(3)</sup>                       | −0.5               | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                                    | V <sub>I</sub> < 0 | −50                   | mA   |
| I <sub>OK</sub>  | Output clamp current                                   | V <sub>O</sub> < 0 | −50                   | mA   |
| I <sub>O</sub>   | Continuous output current                              |                    | ±50                   | mA   |
|                  | Continuous current through each V <sub>CC</sub> or GND |                    | ±100                  | mA   |
| T <sub>stg</sub> | Storage temperature                                    | −65                | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.

### 6.2 ESD Ratings

|                    |                         | VALUE                                                                                    | UNIT |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | 2000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | 1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See <sup>(1)</sup>.

|                 |                                    |                                    | MIN                    | MAX             | UNIT |
|-----------------|------------------------------------|------------------------------------|------------------------|-----------------|------|
| V <sub>CC</sub> | Supply voltage                     |                                    | 1.65                   | 3.6             | V    |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.65 × V <sub>CC</sub> |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2                      |                 |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V | 0.35 × V <sub>CC</sub> |                 | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V   | 0.7                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V to 3.6 V   | 0.8                    |                 |      |
| V <sub>I</sub>  | Input voltage                      |                                    | 0                      | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                     |                                    | 0                      | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V           | −4                     |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | −12                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | −12                    |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V              | −24                    |                 |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V           | 4                      |                 | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V            | 12                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 2.7 V            | 12                     |                 |      |
|                 |                                    | V <sub>CC</sub> = 3 V              | 24                     |                 |      |
| Δt/Δv           | Input transition rise or fall rate |                                    |                        | 10              | ns/V |
| T <sub>A</sub>  | Operating free-air temperature     |                                    | −40                    | 85              | °C   |

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 6.4 Thermal Information<sup>(1)</sup>

| THERMAL METRIC <sup>(1)</sup> |                                        | SN74ALVCH16245                |                               |                             |                                                     |                                                     | UNIT |
|-------------------------------|----------------------------------------|-------------------------------|-------------------------------|-----------------------------|-----------------------------------------------------|-----------------------------------------------------|------|
|                               |                                        | DGG<br>(TSSOP) <sup>(2)</sup> | DGV<br>(TVSOP) <sup>(2)</sup> | DL<br>(SSOP) <sup>(2)</sup> | GQL/ZQL (BGA<br>MICROSTAR<br>JUNIOR) <sup>(2)</sup> | GRD/ZRD (BGA<br>MICROSTAR<br>JUNIOR) <sup>(2)</sup> |      |
|                               |                                        | 48 PINS                       | 48 PINS                       | 48 PINS                     | 56 PINS                                             | 54 PINS                                             |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 70                            | 58                            | 63                          | 42                                                  | 36                                                  | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      | TEST CONDITIONS                                                              | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX | UNIT |
|--------------------------------|------------------------------------------------------------------------------|-----------------|-----------------------|--------------------|-----|------|
| V <sub>OH</sub>                | I <sub>OH</sub> = –100 µA                                                    | 1.65 V to 3.6 V | V <sub>CC</sub> – 0.2 |                    |     | V    |
|                                | I <sub>OH</sub> = –4 mA                                                      | 1.65 V          | 1.2                   |                    |     |      |
|                                | I <sub>OH</sub> = –6 mA                                                      | 2.3 V           | 2                     |                    |     |      |
|                                | I <sub>OH</sub> = –12 mA                                                     | 2.3 V           | 1.7                   |                    |     |      |
|                                |                                                                              | 2.7 V           | 2.2                   |                    |     |      |
|                                |                                                                              | 3 V             | 2.4                   |                    |     |      |
|                                | I <sub>OH</sub> = –24 mA                                                     | 3 V             | 2                     |                    |     |      |
| V <sub>OL</sub>                | I <sub>OL</sub> = 100 µA                                                     | 1.65 V to 3.6 V | 0.2                   |                    |     | V    |
|                                | I <sub>OL</sub> = 4 mA                                                       | 1.65 V          | 0.45                  |                    |     |      |
|                                | I <sub>OL</sub> = 6 mA                                                       | 2.3 V           | 0.4                   |                    |     |      |
|                                | I <sub>OL</sub> = 12 mA                                                      | 2.3 V           | 0.7                   |                    |     |      |
|                                |                                                                              | 2.7 V           | 0.4                   |                    |     |      |
|                                | I <sub>OL</sub> = 24 mA                                                      | 3 V             | 0.55                  |                    |     |      |
| I <sub>I</sub>                 | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           | ±5                    |                    |     | µA   |
| I <sub>I(hold)</sub>           | V <sub>I</sub> = 0.58 V                                                      | 1.65 V          | 25                    |                    |     | µA   |
|                                | V <sub>I</sub> = 1.07 V                                                      | 1.65 V          | –25                   |                    |     |      |
|                                | V <sub>I</sub> = 0.7 V                                                       | 2.3 V           | 45                    |                    |     |      |
|                                | V <sub>I</sub> = 1.7 V                                                       | 2.3 V           | –45                   |                    |     |      |
|                                | V <sub>I</sub> = 0.8 V                                                       | 3 V             | 75                    |                    |     |      |
|                                | V <sub>I</sub> = 2 V                                                         | 3 V             | –75                   |                    |     |      |
|                                | V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>                                   | 3.6 V           | ±500                  |                    |     |      |
| I <sub>OZ</sub> <sup>(3)</sup> | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           | ±10                   |                    |     | µA   |
| I <sub>CC</sub>                | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           | 40                    |                    |     | µA   |
| ΔI <sub>CC</sub>               | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 3.6 V    | 750                   |                    |     | µA   |
| C <sub>i</sub> Control inputs  | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 4                     |                    |     | pF   |
| C <sub>io</sub> A or B ports   | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           | 8                     |                    |     | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7)

| PARAMETER        | FROM (INPUT)           | TO (OUTPUT) | V <sub>CC</sub> = 1.8 V | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     | UNIT |
|------------------|------------------------|-------------|-------------------------|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
|                  |                        |             | TYP                     | MIN                             | MAX | MIN                     | MAX | MIN                             | MAX |      |
| t <sub>pd</sub>  | A or B                 | B or A      | See <sup>(1)</sup>      | 1                               | 3.7 | 3.6                     |     | 1                               | 3   | ns   |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | A or B      | See <sup>(1)</sup>      | 1                               | 5.7 | 5.4                     |     | 1                               | 4.4 | ns   |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | A or B      | See <sup>(1)</sup>      | 1                               | 5.2 | 4.6                     |     | 1                               | 4.1 | ns   |

(1) This information was not available at the time of publication.

## 6.7 Operating Characteristics

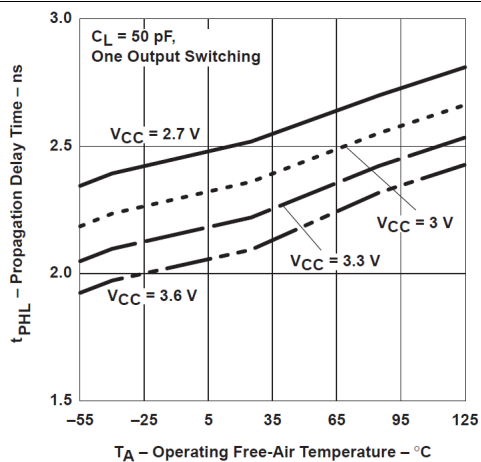
T<sub>A</sub> = 25°C

| PARAMETER                                     |                  | TEST CONDITIONS                    | V <sub>CC</sub> = 1.8 V | V <sub>CC</sub> = 2.5 V | V <sub>CC</sub> = 3.3 V | UNIT |
|-----------------------------------------------|------------------|------------------------------------|-------------------------|-------------------------|-------------------------|------|
|                                               |                  |                                    | TYP                     | TYP                     | TYP                     |      |
| C <sub>pd</sub> Power dissipation capacitance | Outputs enabled  | C <sub>L</sub> = 50 pF, f = 10 MHz | See <sup>(1)</sup>      | 22                      | 29                      | pF   |
|                                               | Outputs disabled |                                    | See <sup>(1)</sup>      | 4                       | 5                       |      |

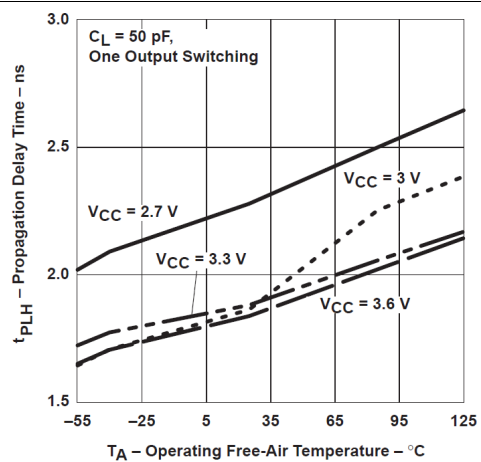
(1) This information was not available at the time of publication.



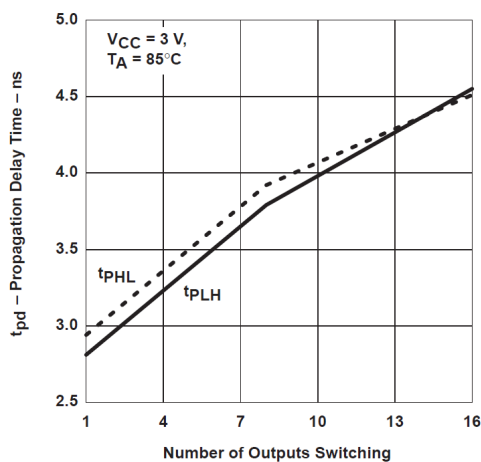
## 6.8 Typical Characteristics



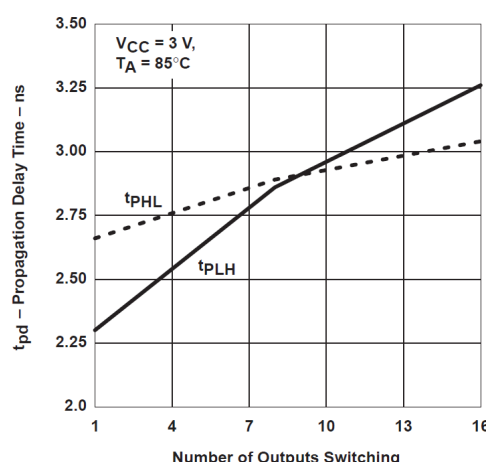
**Figure 1. Propagation Delay Time vs Operating Free-Air Temperature**



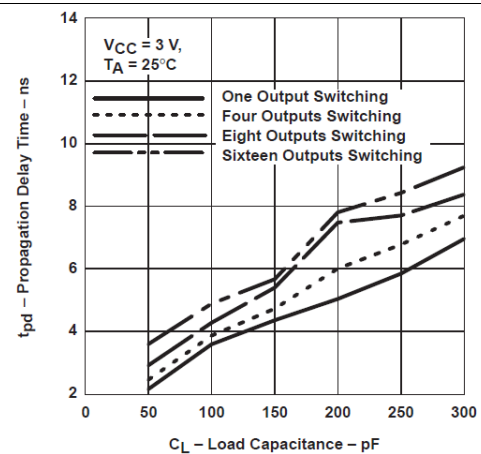
**Figure 2. Propagation Delay Time vs Operating Free-Air Temperature**



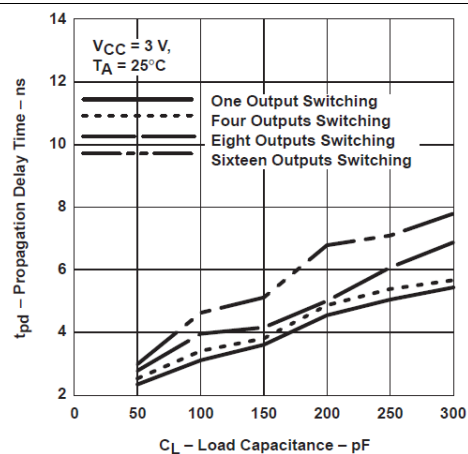
**Figure 3. Propagation Delay Time vs Number of Outputs Switching**



**Figure 4. Propagation Delay Time vs Number of Outputs Switching**

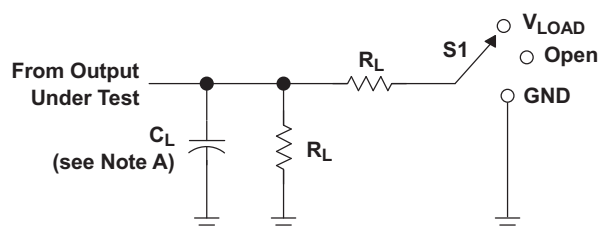


**Figure 5. Propagation Delay Time vs Load Capacitance**



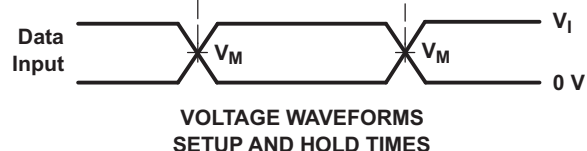
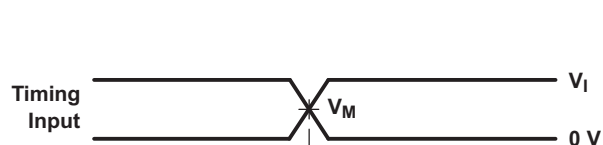
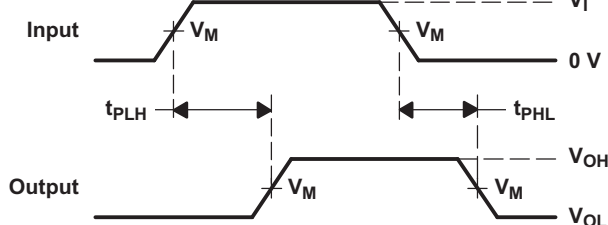
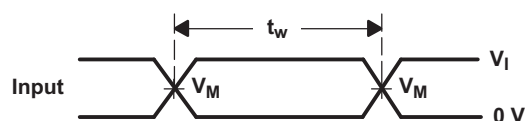
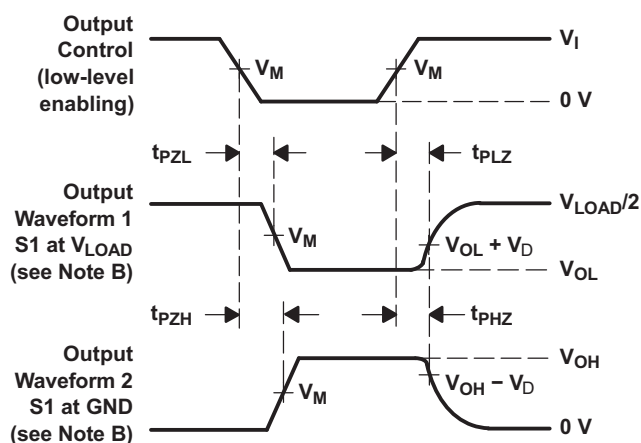
**Figure 6. Propagation Delay Time vs Load Capacitance**

## 7 Parameter Measurement Information


**LOAD CIRCUIT**

| TEST              | S1         |
|-------------------|------------|
| $t_{pd}$          | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PHL}$ | GND        |

| $V_{CC}$                          | INPUT    |               | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_D$  |
|-----------------------------------|----------|---------------|------------|-------------------|-------|--------------|--------|
|                                   | $V_I$    | $t_r/t_f$     |            |                   |       |              |        |
| 1.8 V                             | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V |
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | $V_{CC}$ | $\leq 2$ ns   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V |
| 2.7 V                             | 2.7 V    | $\leq 2.5$ ns | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V  |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 2.7 V    | $\leq 2.5$ ns | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V  |


**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 7. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

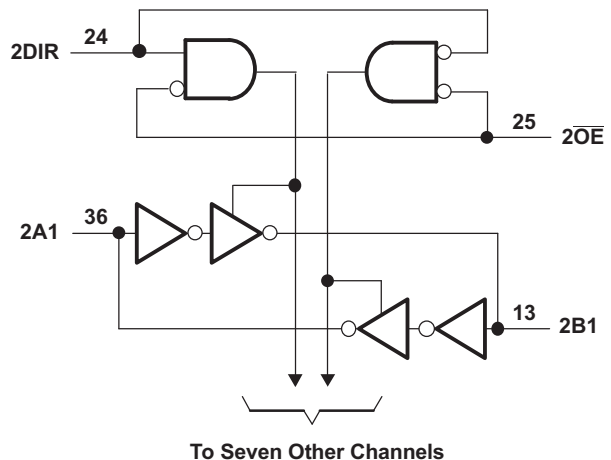
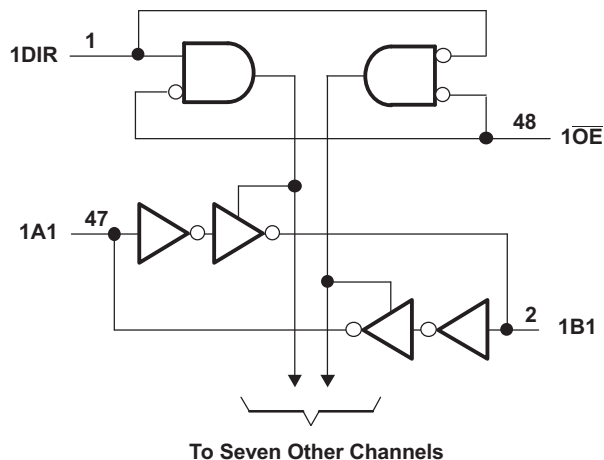
## 8.1 Overview

The SN74ALVCH16245 device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic high or low level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

## 8.2 Functional Block Diagrams



### 8.3 Feature Description

The input tolerance of 5.5V inputs allows the device to be used in down voltage translation applications as well for example if translation is required from 5 V to 3.3 V or 1.8 V. Also bus hold on data inputs eliminates the need for external pullup or pulldown resistors to be used, enabling customer to save board space and system cost.

## 8.4 Device Functional Modes

Table 1 lists the functional modes for SN74ALVCH16245.

### Table 1. Function Table

| INPUTS                 |     | OPERATION       |
|------------------------|-----|-----------------|
| $\overline{\text{OE}}$ | DIR |                 |
| L                      | L   | B data to A bus |
| L                      | H   | A data to B bus |
| H                      | X   | Isolation       |

## 9 Application and Implementation

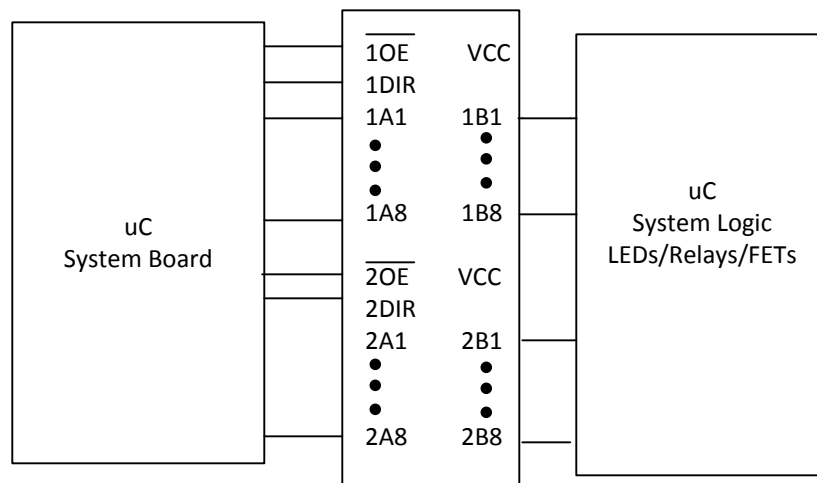
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

SN74ALVCH16245A is a high-drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making it ideal for down translation.

### 9.2 Typical Application



**Figure 8. Typical Application Schematic**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specification, see [Switching Characteristics](#)
  - For specified high and low levels, see ( $V_{IH}$  and  $V_{IL}$ ) in the [Electrical Characteristics](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  max) in the [Absolute Maximum Ratings](#) table at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed ( $I_O$  max) per output and should not exceed (Continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Recommended Operating Conditions](#) table.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 9.2.3 Application Curves

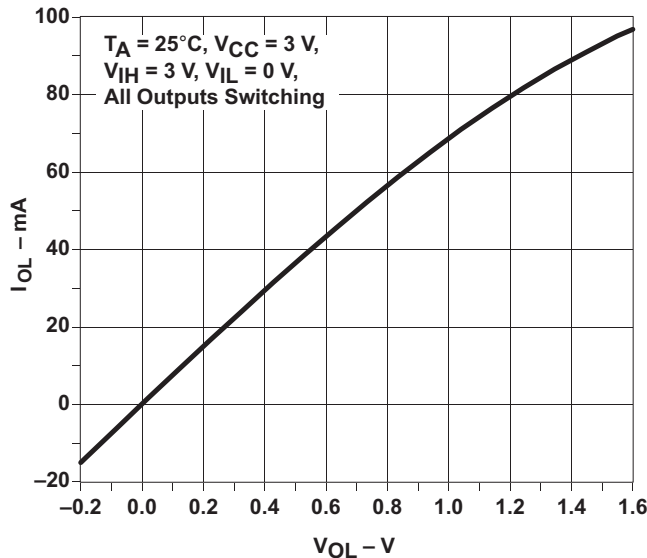


Figure 9. Output Drive Current ( $I_{OL}$ ) vs LOW-level Output Voltage ( $V_{OL}$ )

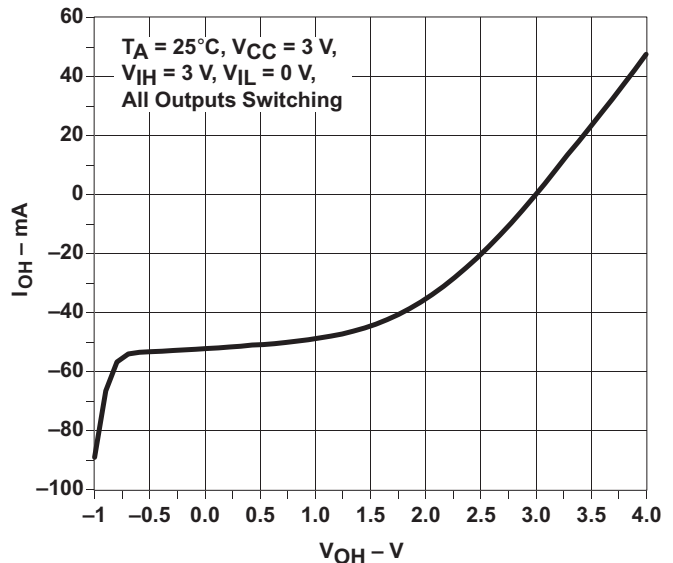


Figure 10. Output Drive Current ( $I_{OH}$ ) vs HIGH-level Output Voltage ( $V_{OH}$ )

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Absolute Maximum Ratings](#) table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single-supply, a 0.1- $\mu\text{F}$  capacitor is recommended. If there are multiple  $V_{CC}$  terminals then 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 11](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient.

### 11.2 Layout Example

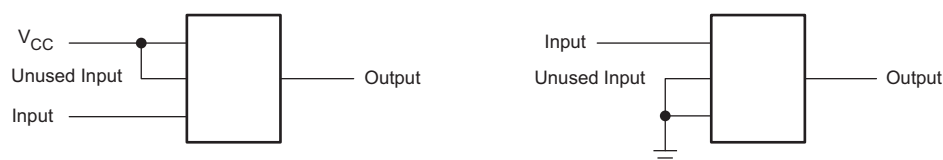


Figure 11. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

Widebus, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| 74ALVCH16245DGGRG4                 | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH16245          |
| 74ALVCH16245DGVRG4                 | Active        | Production           | TVSOP (DGV)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VH245               |
| 74ALVCH16245DGVRG4.B               | Active        | Production           | TVSOP (DGV)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VH245               |
| <a href="#">SN74ALVCH16245DGGR</a> | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH16245          |
| SN74ALVCH16245DGGR.B               | Active        | Production           | TSSOP (DGG)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH16245          |
| <a href="#">SN74ALVCH16245DGVR</a> | Active        | Production           | TVSOP (DGV)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VH245               |
| SN74ALVCH16245DGVR.B               | Active        | Production           | TVSOP (DGV)   48 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | VH245               |
| <a href="#">SN74ALVCH16245DL</a>   | Active        | Production           | SSOP (DL)   48   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH16245          |
| SN74ALVCH16245DL.B                 | Active        | Production           | SSOP (DL)   48   | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH16245          |
| <a href="#">SN74ALVCH16245DLR</a>  | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH16245          |
| SN74ALVCH16245DLR.B                | Active        | Production           | SSOP (DL)   48   | 1000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ALVCH16245          |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74ALVCH16245 :**

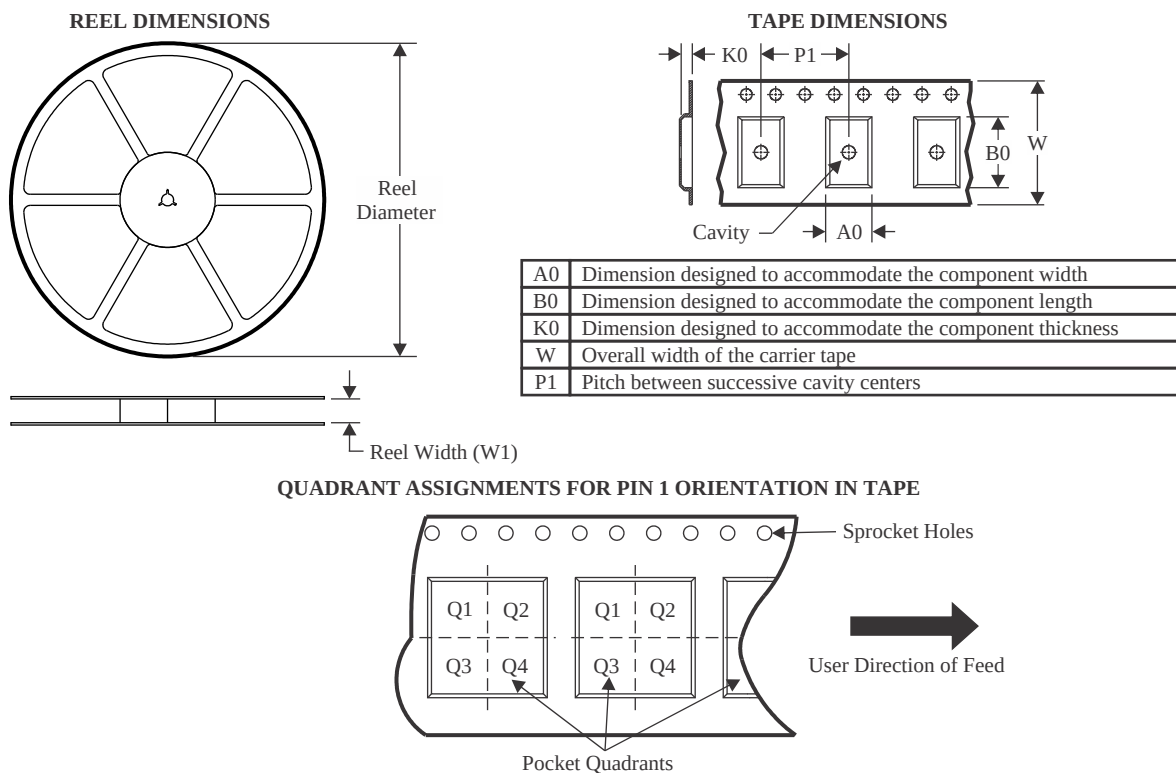
- Enhanced Product : [SN74ALVCH16245-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications



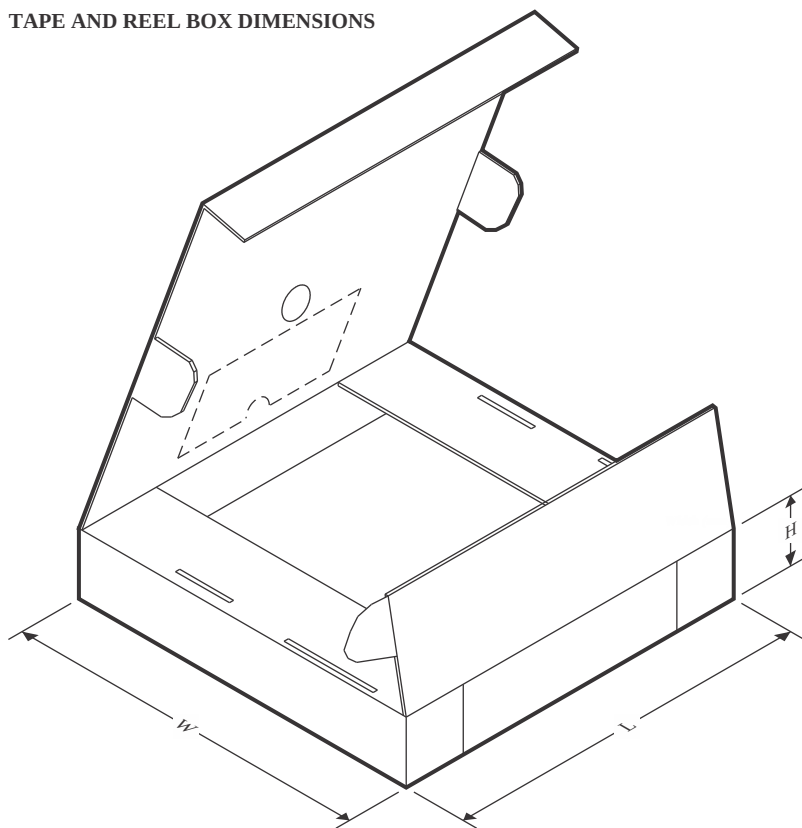
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74ALVCH16245DGVRG4 | TVSOP        | DGV             | 48   | 2000 | 330.0              | 16.4               | 7.1     | 10.2    | 1.6     | 12.0    | 16.0   | Q1            |
| SN74ALVCH16245DGGR | TSSOP        | DGG             | 48   | 2000 | 330.0              | 24.4               | 8.6     | 13.0    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74ALVCH16245DGVR | TVSOP        | DGV             | 48   | 2000 | 330.0              | 16.4               | 7.1     | 10.2    | 1.6     | 12.0    | 16.0   | Q1            |
| SN74ALVCH16245DLR  | SSOP         | DL              | 48   | 1000 | 330.0              | 32.4               | 11.35   | 16.2    | 3.1     | 16.0    | 32.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74ALVCH16245DGVRG4 | TVSOP        | DGV             | 48   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ALVCH16245DGGR | TSSOP        | DGG             | 48   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74ALVCH16245DGVR | TVSOP        | DGV             | 48   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ALVCH16245DLR  | SSOP         | DL              | 48   | 1000 | 367.0       | 367.0      | 55.0        |

## TUBE

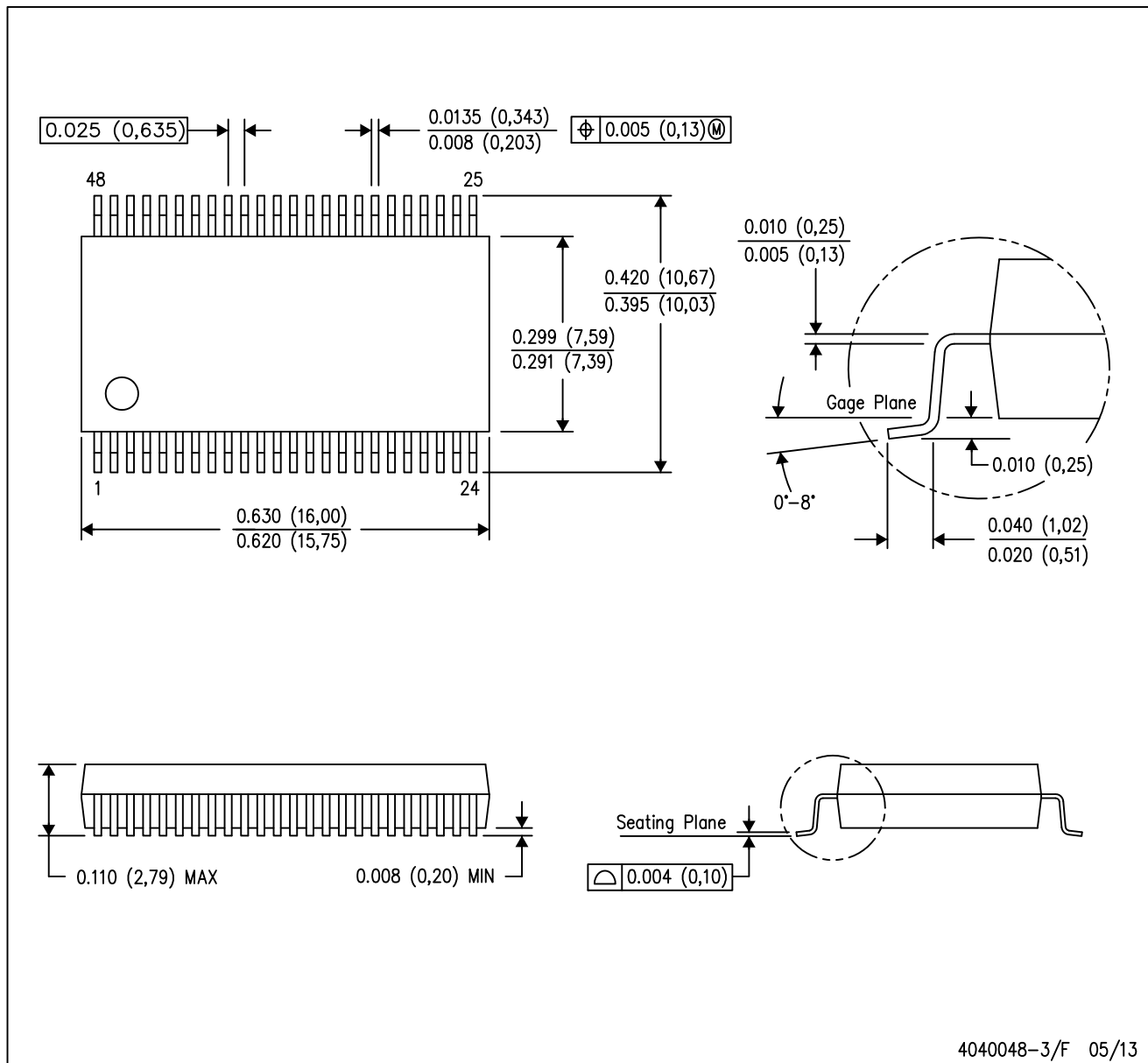


\*All dimensions are nominal

| Device             | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ALVCH16245DL   | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |
| SN74ALVCH16245DL.B | DL           | SSOP         | 48   | 25  | 473.7  | 14.24  | 5110   | 7.87   |

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

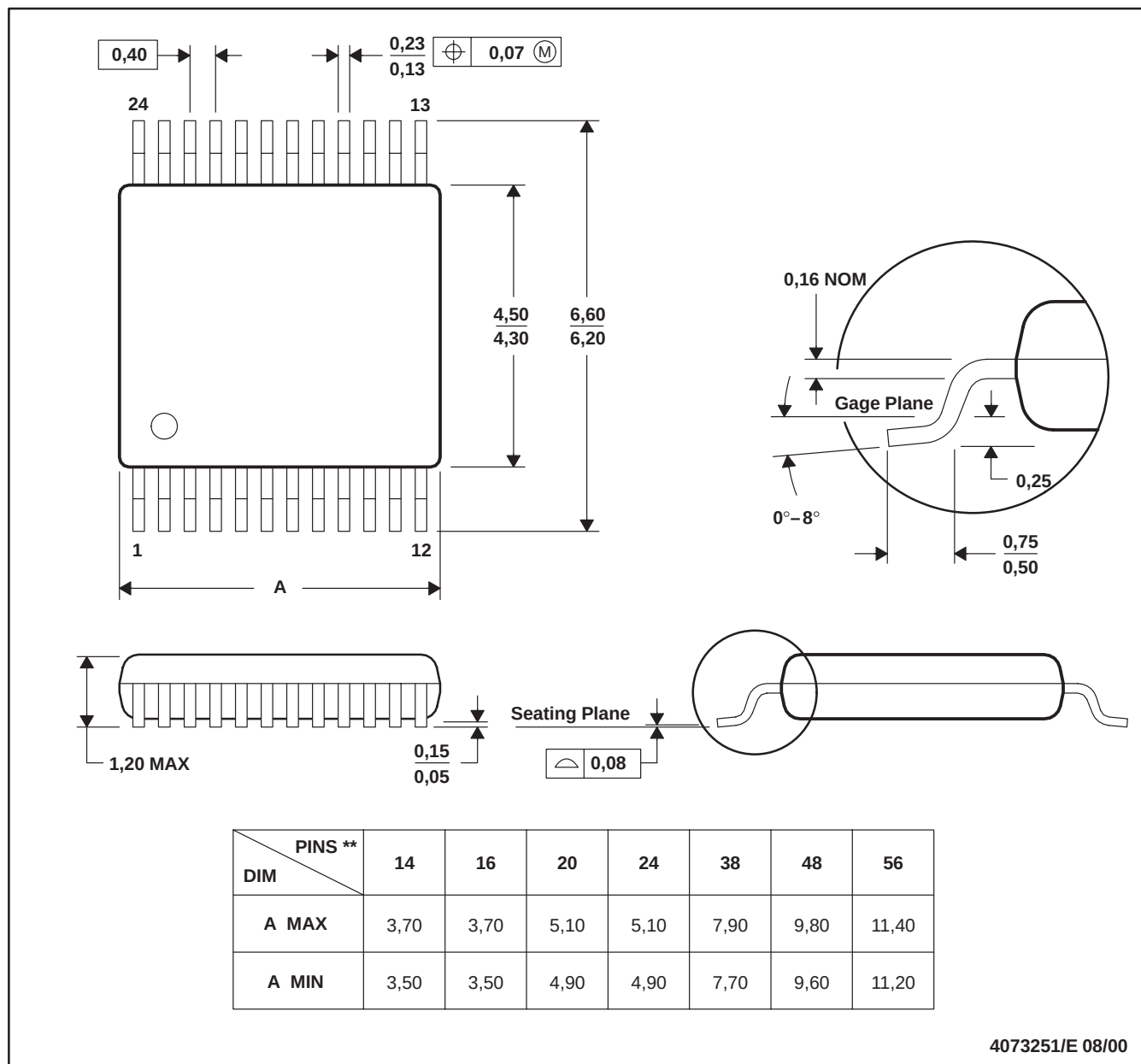


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

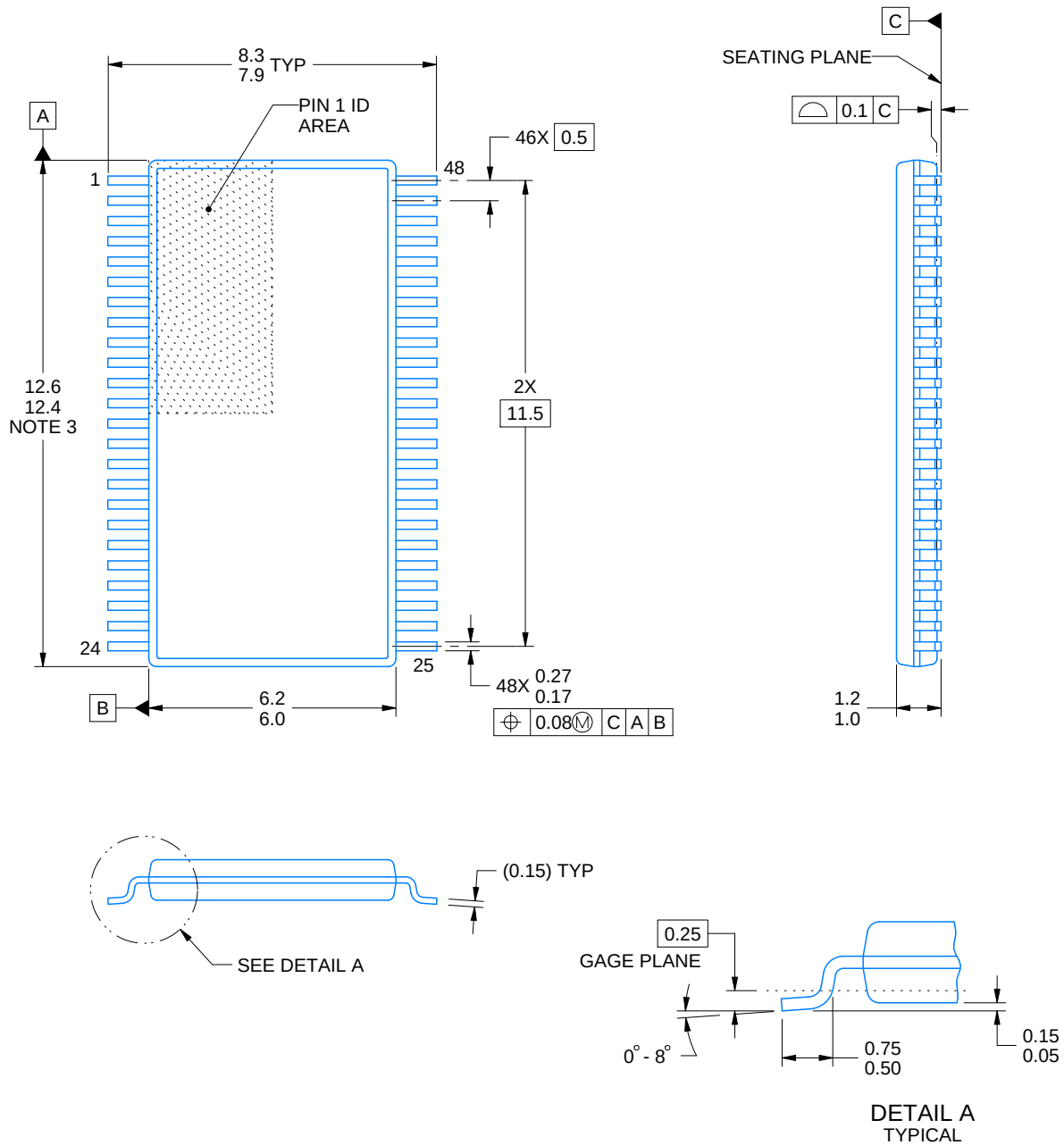
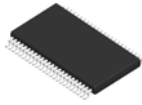
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



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## NOTES:

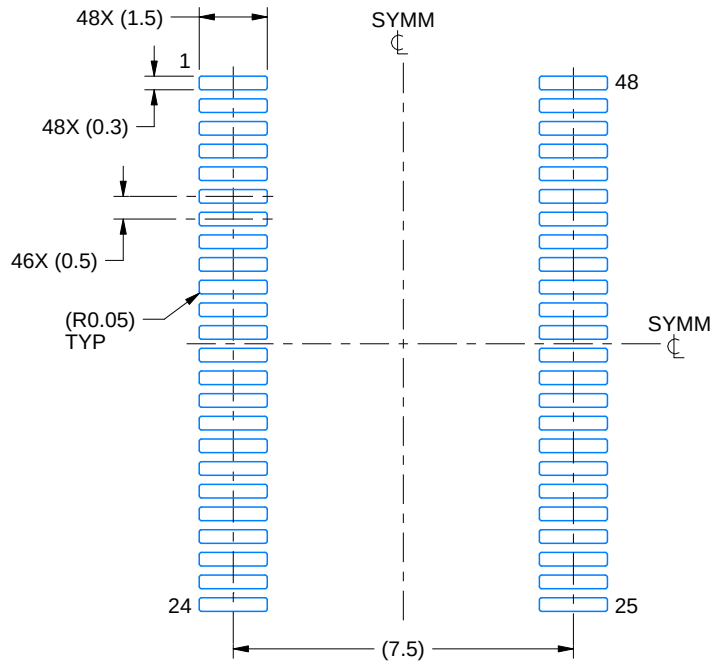
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

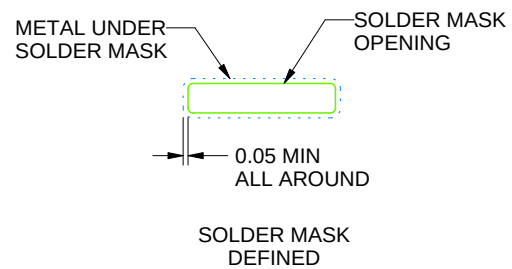
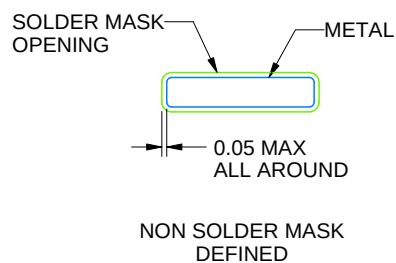
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

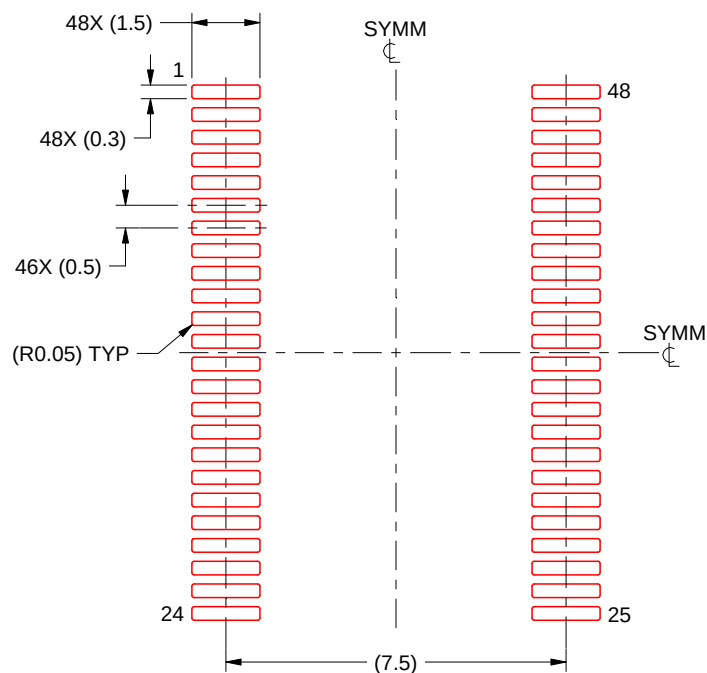
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

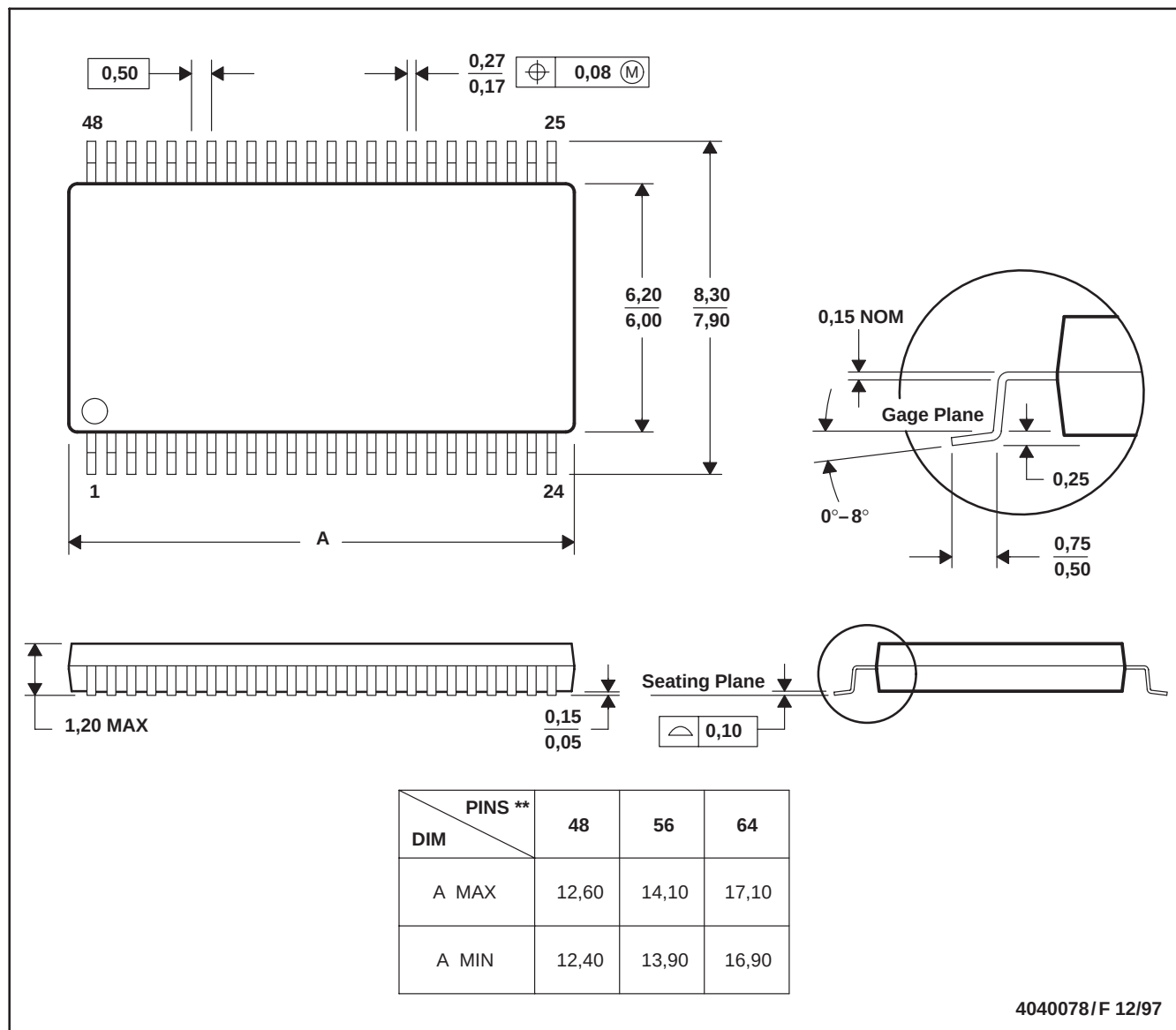
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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