

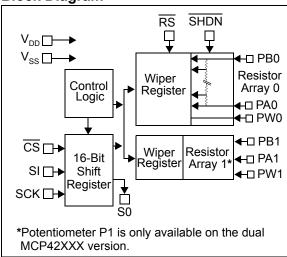
MCP41XXX/42XXX

Single/Dual Digital Potentiometer with SPITM Interface

Features

- · 256 taps for each potentiometer
- Potentiometer values for 10 k Ω , 50 k Ω and 100 k Ω
- · Single and dual versions
- SPI™ serial interface (mode 0,0 and 1,1)
- · ±1 LSB max INL & DNL
- · Low power CMOS technology
- 1 µA maximum supply current in static operation
- Multiple devices can be daisy-chained together (MCP42XXX only)
- Shutdown feature open circuits of all resistors for maximum power savings
- Hardware shutdown pin available on MCP42XXX only
- Single supply operation (2.7V 5.5V)
- Industrial temperature range: -40°C to +85°C
- Extended temperature range: -40°C to +125°C

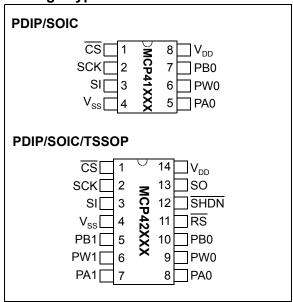
Block Diagram



Description

The MCP41XXX and MCP42XXX devices are 256position, digital potentiometers available in 10 k Ω , 50 k Ω and 100 k Ω resistance versions. MCP41XXX is a single-channel device and is offered in an 8-pin PDIP or SOIC package. The MCP42XXX contains two independent channels in a 14-pin PDIP, SOIC TSSOP package. The wiper position of the MCP41XXX/42XXX varies linearly and is controlled via an industry-standard SPI interface. The devices consume <1 µA during static operation. A software shutdown feature is provided that disconnects the "A" terminal from the resistor stack and simultaneously connects the wiper to the "B" terminal. In addition, the dual MCP42XXX has a SHDN pin that performs the same function in hardware. During shutdown mode, the contents of the wiper register can be changed and the potentiometer returns from shutdown to the new value. The wiper is reset to the mid-scale position (80h) upon power-up. The \overline{RS} (reset) pin implements a hardware reset and also returns the wiper to mid-scale. The MCP42XXX SPI interface includes both the SI and SO pins, allowing daisy-chaining of multiple devices. Channel-to-channel resistance matching on the MCP42XXX varies by less than 1%. These devices operate from a single 2.7 - 5.5V supply and are specified over the extended and industrial temperature ranges.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS: 10 $k\Omega$ VERSION

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +2.7V$ to 5.5V, $T_A = -40^{\circ}\text{C}$ to +85°C (TSSOP devices are only specified at +25°C and +85°C). Typical specifications represent values for $V_{DD} = 5V$, $V_{SS} = 0V$, $V_B = 0V$, $T_A = +25^{\circ}\text{C}$.

+85°C). Typical specifications represent v	Sym	Min	Тур	Max	Units	Conditions
Rheostat Mode		1	.74		2.110	253110110
Nominal Resistance	R	8	10	12	kΩ	T _A = +25°C (Note 1)
Rheostat Differential Non Linearity	R-DNL	-1	±1/4	+1	LSB	Note 2
Rheostat Integral Non Linearity	R-INL	-1	±1/4	+1	LSB	Note 2
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	_	800	_	ppm/°C	11010 2
Wiper Resistance	R _W	_	52	100	Ω	V _{DD} = 5.5V, I _W = 1 mA, code 00h
Wipor Redictarios	R _W	_	73	125	Ω	V _{DD} = 2.7V, I _W = 1 mA, code 00h
Wiper Current	I _W	-1	_	+1	mA	
Nominal Resistance Match	ΔR/R	_	0.2	1	%	MCP42010 only, P0 to P1; T _A = +25°C
Potentiometer Divider	2.0.0		0.2	·	,,	
Resolution	N	8	_	_	Bits	
Monotonicity	N	8	_		Bits	
Differential Non-Linearity	DNL	-1	±1/4	+1	LSB	Note 3
Integral Non-Linearity	INL	-1	±1/4	+1	LSB	Note 3
Voltage Divider Tempco	$\Delta V_W/\Delta T$	_	1		ppm/°C	Code 80h
Full Scale Error	V _{WFSE}	-2	-0.7	0	LSB	Code FFh, V _{DD} = 5V, see Figure 2-25
	V _{WFSE}	-2	-0.7	0	LSB	Code FFh, V _{DD} = 3V, see Figure 2-25
Zero Scale Error	V _{WZSE}	0	+0.7	+2	LSB	Code 00h, V _{DD} = 5V, see Figure 2-25
	V _{WZSE}	0	+0.7	+2	LSB	Code 00h, V _{DD} = 3V, see Figure 2-25
Resistor Terminals	WZSE					
Voltage Range	$V_{A,B,W}$	0	_	V_{DD}		Note 4
Capacitance (C _A or C _B)	Α,υ,••	_	15	_	pF	f = 1 MHz, Code = 80h, see Figure 2-30
Capacitance	C _w	_	5.6		pF	f = 1 MHz, Code = 80h, see Figure 2-30
Dynamic Characteristics (All dynamic		ics use V _{DE}	, = 5V)			, , , , , , , , , , , , , , , , , , , ,
Bandwidth -3dB	BW	_	1	_	MHz	V _B = 0V, Measured at Code 80h,
						Output Load = 30 PF
Settling Time	t _S	_	2	_	μS	$V_A = V_{DD}, V_B = 0V, \pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF
Resistor Noise Voltage	e _{NWB}	_	9		nV/√ Hz	V _A = Open, Code 80h, f =1 kHz
Crosstalk	C_{T}		-95		dB	$V_A = V_{DD}, V_B = 0V$ (Note 5)
Digital Inputs/Outputs (CS, SCK, SI, SC	O) See Figure	2-12 for R	S and SHI	ON pin ope	ration	
Schmitt Trigger High-Level Input Voltage	V _{IH}	0.7V _{DD}	_	_	V	
Schmitt Trigger Low-Level Input Voltage	V _{IL}	_	_	$0.3V_{DD}$	V	
Hysteresis of Schmitt Trigger Inputs	V _{HYS}	_	0.05V _{DD}	_		
Low-Level Output Voltage	V _{OL}	_	_	0.40	V	I _{OL} = 2.1 mA, V _{DD} = 5V
High-Level Output Voltage	V _{OH}	V _{DD} - 0.5	_		V	I _{OH} = -400 μA, V _{DD} = 5V
Input Leakage Current	I _{LI}	-1	_	+1	μΑ	$\overline{\text{CS}} = V_{\text{DD}}, V_{\text{IN}} = V_{\text{SS}} \text{ or } V_{\text{DD}}, \text{ includes } V_{\text{A}} \overline{\text{SHDN}} = 0$
Pin Capacitance (All inputs/outputs)	C _{IN} , C _{OUT}	_	10	_	pF	V_{DD} = 5.0V, T_A = +25°C, f_c = 1 MHz
Power Requirements						
Operating Voltage Range	V_{DD}	2.7	_	5.5	V	
Supply Current, Active	I _{DDA}	_	340	500	μA	V_{DD} = 5.5V, \overline{CS} = V_{SS} , f_{SCK} = 10 MHz, SO = Open, Code FFh (Note 6)
Supply Current, Static	I _{DDS}	_	0.01	1	μA	CS, SHDN, RS = V _{DD} = 5.5V, SO = Open (Note 6)
Power Supply Sensitivity	PSS	_	0.0015	0.0035	%/%	V _{DD} = 4.5V - 5.5V, V _A = 4.5V, Code 80h
	PSS	_	0.0015	0.0035	%/%	V _{DD} = 2.7V - 3.3V, V _A = 2.7V, Code 80h

Note 1: $V_{AB} = V_{DD}$, no connection on wiper.

^{2:} Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. I_W = 50 μA for V_{DD} = 3V and I_W = 400 μA for V_{DD} = 5V for 10 kΩ version. See Figure 2-26 for test circuit.

^{3:} INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. V_A = V_{DD} and V_B = 0V. DNL specification limits of ±1 LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.

^{4:} Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full-scale and zero-scale error were measured using Figure 2-25.

Measured at V_W pin where the voltage on the adjacent V_W pin is swinging full-scale.

^{6:} Supply current is independent of current through the potentiometers.

DC CHARACTERISTICS: 50 kΩ VERSION

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C (TSSOP devices are only specified at +25°C and +85°C). Typical specifications represent values for V_{DD} = 5V, V_{SS} = 0V, V_{B} = 0V, V_{A} = +25°C.

+85°C). Typical specifications represent values for V _{DD} = 5V, V _{SS} = 0V, V _B = 0V, T _A = +25°C.										
Parameters	Sym	Min	Тур	Max	Units	Conditions				
Rheostat Mode										
Nominal Resistance	R	35	50	65	kΩ	$T_A = +25^{\circ}C$ (Note 1)				
Rheostat Differential Non-Linearity	R-DNL	-1	±1/4	+1	LSB	Note 2				
Rheostat Integral Non-Linearity	R-INL	-1	±1/4	+1	LSB	Note 2				
Rheostat Tempco	$\Delta R_{AB}/\Delta T$	_	800	_	ppm/°C					
Wiper Resistance	R_W	-	125	175	Ω	V_{DD} = 5.5V, I_{W} = 1 mA, code 00h				
	R_W	_	175	250	Ω	$V_{DD} = 2.7V$, $I_{W} = 1$ mA, code 00h				
Wiper Current	I _W	-1	-	+1	mA					
Nominal Resistance Match	ΔR/R	ı	0.2	1	%	MCP42050 only, P0 to P1;T _A = +25°C				
Potentiometer Divider										
Resolution	Ν	8		I	Bits					
Monotonicity	N	8		-	Bits					
Differential Non-Linearity	DNL	-1	±1/4	+1	LSB	Note 3				
Integral Non-Linearity	INL	-1	±1/4	+1	LSB	Note 3				
Voltage Divider Tempco	$\Delta V_W/\Delta T$	_	1	_	ppm/°C	Code 80h				
Full-Scale Error	V _{WFSE}	-1	-0.25	0	LSB	Code FFh, V _{DD} = 5V, see Figure 2-25				
	V _{WFSE}	-1	-0.35	0	LSB	Code FFh, V _{DD} = 3V, see Figure 2-25				
Zero-Scale Error	V _{WZSE}	0	+0.25	+1	LSB	Code 00h, V _{DD} = 5V, see Figure 2-25				
	V _{WZSE}	0	+0.35	+1	LSB	Code 00h, V _{DD} = 3V, see Figure 2-25				
Resistor Terminals										
Voltage Range	$V_{A,B,W}$	0	_	V_{DD}		Note 4				
Capacitance (C _A or C _B)		_	11	_	pF	f =1 MHz, Code = 80h, see Figure 2-30				
Capacitance	C _W		5.6		pF	f =1 MHz, Code = 80h, see Figure 2-30				
Dynamic Characteristics (All dynamic	characteristi	cs use V _{DE}) = 5V)							
Bandwidth -3dB	BW	_	280	_	MHz	V _B = 0V, Measured at Code 80h, Output Load = 30 PF				
Settling Time	t _S	_	8	_	μS	$V_A = V_{DD}, V_B = 0V, \pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF				
Resistor Noise Voltage	e _{NWB}	_	20	_	nV/√Hz	V _A = Open, Code 80h, f =1 kHz				
Crosstalk	C _T	_	-95	_	dB	$V_A = V_{DD}$, $V_B = 0V$ (Note 5)				
Digital Inputs/Outputs (CS, SCK, SI, SC	O) See Figure	2-12 for R	S and SHE	ON pin ope	ration.					
Schmitt Trigger High-Level Input Voltage	V _{IH}	0.7V _{DD}	_		V					
Schmitt Trigger Low-Level Input Voltage	V_{IL}	_	_	0.3V _{DD}	V					
Hysteresis of Schmitt Trigger Inputs	V _{HYS}	_	0.05V _{DD}	_						
Low-Level Output Voltage	V _{OL}	_	_	0.40	V	I _{OL} = 2.1 mA, V _{DD} = 5V				
High-Level Output Voltage	V _{OH}	V _{DD} - 0.5	_		V	I _{OH} = -400 μA, V _{DD} = 5V				
Input Leakage Current	ILI	-1	_	+1	μA	$\overline{\text{CS}} = \text{V}_{\text{DD}}, \text{V}_{\text{IN}} = \text{V}_{\text{SS}} \text{ or } \text{V}_{\text{DD}}, \text{ includes } \text{V}_{\text{A}} \overline{\text{SHDN}} = 0$				
Pin Capacitance (All inputs/outputs)	C _{IN} , C _{OUT}	_	10	_	pF	V _{DD} = 5.0V, T _A = +25°C, f _c = 1 MHz				
Power Requirements	551					· · · ·				
Operating Voltage Range	V_{DD}	2.7	_	5.5	V					
Supply Current, Active	I _{DDA}	_	340	500	μA	V _{DD} = 5.5V, CS = V _{SS} , f _{SCK} = 10 MHz, SO = Open, Code FFh (Note 6)				
Supply Current, Static	I _{DDS}	_	0.01	1	μA	$\overline{\text{CS}}$, $\overline{\text{SHDN}}$, $\overline{\text{RS}}$ = V_{DD} = 5.5V, SO = Open (Note 6)				
Power Supply Sensitivity	PSS	_	0.0015	0.0035	%/%	V _{DD} = 4.5V - 5.5V, V _A = 4.5V, Code 80h				
,	PSS	_	0.0015	0.0035	%/%	V _{DD} = 2.7V - 3.3V, V _A = 2.7V, Code 80h				
L						DD, A, TTTTT				

Note

- 1:
- $V_{AB} = V_{DD}$, no connection on wiper. Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. $I_W = V_{DD}/R$ for +3V or +5V for 50 $k\Omega$ version. See Figure 2-26 for test circuit.
- INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. $V_A = V_{DD}$ and $V_B = 0V$. DNL specification limits of ±1 LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.
- Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full-scale and zero-scale error were measured
- Measured at V_W pin where the voltage on the adjacent V_W pin is swinging full scale.
- Supply current is independent of current through the potentiometers.

DC CHARACTERISTICS: 100 k Ω VERSION

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.7V to 5.5V, T_A = -40°C to +85°C (TSSOP devices are only specified at +25°C and +85°C). Typical specifications represent values for V_{DD} = 5V, V_{SS} = 0V, V_B = 0V, T_A = +25°C.

$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	+85°C). Typical specifications represent values for V _{DD} = 5V, V _{SS} = 0V, V _B = 0V, T _A = +25°C.										
Nominal Resistance R 70 100 130 KΩ T _A = 25°C (Note 1)	Parameters	Sym	Min	Тур	Max	Units	Conditions				
Renostat Differential Non-Linearity R-DNL -1 ±1/4 +1 LSB Note 2	Rheostat Mode										
Rheostat Integral Non-Linearity R-INL -1 ±1/4 +1 LSB Note 2	Nominal Resistance	R	70	100	130	kΩ	T _A = +25°C (Note 1)				
Repeated Tempoo AR _{AB} /ΔT 800 ppm/°C	Rheostat Differential Non-Linearity	R-DNL	-1	±1/4	+1	LSB	Note 2				
Wigher Resistance	Rheostat Integral Non-Linearity	R-INL	-1	±1/4	+1	LSB	Note 2				
Note 3	Rheostat Tempco	$\Delta R_{AB}/\Delta T$	_	800		ppm/°C					
Wight Current Iw -1 -	Wiper Resistance	R_W	_	125	175	Ω	V_{DD} = 5.5V, I_{W} = 1 mA, code 00h				
Nominal Resistance Match AR/R 0.2 1 % MCP42010 only, P0 to P1; T _A = +25°C Potentiometer Divider		R_W	_	175	250	Ω	V_{DD} = 2.7V, I_{W} = 1 mA, code 00h				
Resolution	Wiper Current	I _W	-1	_	+1	mA					
Resolution	Nominal Resistance Match	ΔR/R	_	0.2	1	%	MCP42010 only, P0 to P1;T _A = +25°C				
Monotonicity N 8 Bits Differential Non-Linearity DNL -1 ±1/4 +1 LSB Note 3	Potentiometer Divider										
Differential Non-Linearity DNL -1 ±1/4 +1 LSB Note 3	Resolution	N	8	_		Bits					
Integral Non-Linearity	Monotonicity	N	8	_		Bits					
Voltage Divider Tempto ΔV _W /ΔT −− 1 −− ppm/"C Code 80h	Differential Non-Linearity	DNL	-1	±1/4	+1	LSB	Note 3				
Full-Scale Error	Integral Non-Linearity	INL	-1	±1/4	+1	LSB	Note 3				
V _{WFSE} 1 0.35 0 LSB Code FFh, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.25 +1 LSB Code 00h, V _{DD} = 5V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 5V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 3V, see Figure 2-25 V _{WZSE} 0 +0.35 +1 LSB Code 00h, V _{DD} = 8V, see Figure 2-25 V _{WZSE} 0 +0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.56 -0 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.50 -0.50 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.50 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.50 pF f =1 MHz, Code = 80h, see Figure 2-30 V _{WZSE} 0 -0.50 pF f =1 MHz, Co	Voltage Divider Tempco	$\Delta V_W/\Delta T$	_	1	_	ppm/°C	Code 80h				
Vivilia Viv	Full-Scale Error	V _{WFSE}	-1	-0.25	0	LSB	Code FFh, V _{DD} = 5V, see Figure 2-25				
Resistor Terminals Voltage Range VA,B,W 0 — VDD Note 4 Capacitance (CA or CB) — 111 — pF f =1 MHz, Code = 80h, see Figure 2-30 Capacitance CW — 5.6 — pF f =1 MHz, Code = 80h, see Figure 2-30 Dynamic Characteristics (All dynamic characteristics use V _{DD} = 5V.) BMW — 145 — MHZ V _B = 0V. Measured at Code 80h, Output Load = 30 PF Settling Time t _S — 18 — µS V _A = V _{DD} , V _B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 PF Resistor Noise Voltage e _{NWB} — 29 — nN/HZ V _A = V _{DD} , V _B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF Resistor Noise Voltage e _{NWB} — 29 — nN/HZ V _A = Open, Code 80h, F=1 kHz Crosstalk C _T — -95 — dB V _A = V _{DD} , V _B = 0V (Note 5) Bigital Inputs/Outputs (CS, SCK, SI, SO, SS, KS, SI, SO, SS er Figure 2-12 for RS and SHDN pin operation. SCHINGT Trigger Input SUMD (Note 5) — —		V_{WFSE}	-1	-0.35	0	LSB	Code FFh, V _{DD} = 3V, see Figure 2-25				
Note	Zero-Scale Error	V_{WZSE}	0	+0.25	+1	LSB	Code 00h, V _{DD} = 5V, see Figure 2-25				
Voltage Range		V _{WZSE}	0	+0.35	+1	LSB	Code 00h, V _{DD} = 3V, see Figure 2-25				
Capacitance (CA or CB) — 11 — pF f = 1 MHz, Code = 80h, see Figure 2-30 Capacitance C _W — 5.6 — pF f = 1 MHz, Code = 80h, see Figure 2-30 Dynamic Characteristics (All dynamic characteristics use V _{DD} = 5V.) Bandwidth -3dB BW — 145 — MHz V _B = 0V, Measured at Code 80h, Output Load = 30 pF Settling Time Is — 18 — µS V _A = V _{DD} , V _B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF Resistor Noise Voltage e _{NWB} — 29 — nV/Hz V _A = Open, Code 80h, f = 1 kHz Crosstalk C _T — 95 — dB V _A = V _{DD} , V _B = 0V (Note 5) Digital Inputs/Outputs (CS, SCK, SI, SO) See Figure 2-12 for RS and SHDN pin operation. Schmitt Trigger Hight-Level Input Voltage V _{IH} 0.7V _{DD} — — V Schmitt Trigger Low-Level Input Voltage V _{IL} — — 0.3V _{DD} V Hysteresis of Schmitt Trigger Inputs V _{HYS} — 0.05V _{DD} — —	Resistor Terminals										
Capacitance C _W - 5.6 - pF f = 1 MHz, Code = 80h, see Figure 2-30 Dynamic Characteristics (All dynamic characteristics use V _{DD} = 5V.) Bandwidth -3dB BW - 145 - MHz V _B = 0V, Measured at Code 80h, Output Load = 30 PF Settling Time t _S - 18 - µS V _A = V _{DD} , V _B = 0V, ±1% Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF Resistor Noise Voltage e _{NWB} - 29 - nV/Hz V _A = Open, Code 80h, f = 1 kHz Crosstalk C _T - -95 - dB V _A = V _{DD} , V _B = 0V (Note 5) Digital Inputs/Outputs (CS, SCK, SI, SO) See Figure 2-12 for RS and SHDN pin operation. Schmitt Trigger High-Level Input Voltage V _{IL} - - V Schmitt Trigger Low-Level Input Voltage V _{IL} - - 0.05V _{DD} - V Hysteresis of Schmitt Trigger Inputs V _{HYS} - 0.05V _{DD} - - V Low-Level Output Voltage V _{OL} - - 0.40 V I _{OL}	Voltage Range	$V_{A,B,W}$	0	_	V_{DD}		Note 4				
Dynamic Characteristics (All dynamic characteristics use V _{DD} = 5V.) Bandwidth -3dB	Capacitance (CA or CB)		_	11	_	pF	f =1 MHz, Code = 80h, see Figure 2-30				
Bandwidth -3dB			_		_	pF	f =1 MHz, Code = 80h, see Figure 2-30				
Settling Time $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Dynamic Characteristics (All dynamic	characterist	ics use V _{DE}) = 5V.)							
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Bandwidth -3dB	BW	_	145	1	MHz	V _B = 0V, Measured at Code 80h, Output Load = 30 PF				
Crosstalk C _T - -95 - dB V _A = V _{DD} , V _B = 0V (Note 5) Digital Inputs/Outputs (CS, SCK, SI, SO) See Figure 2-12 for RS and SHDN pin operation. Schmitt Trigger High-Level Input Voltage V _{IH} 0.7V _{DD} - - V Schmitt Trigger Low-Level Input Voltage V _{IL} - - 0.3V _{DD} V Hysteresis of Schmitt Trigger Inputs V _{HYS} - 0.05V _{DD} - - Low-Level Output Voltage V _{OL} - - 0.40 V I _{OL} = 2.1 mA, V _{DD} = 5V High-Level Output Voltage V _{OL} - - - V I _{OL} = -400 μA, V _{DD} = 5V Input Leakage Current I _{LI} -1 - +1 μA CS = V _{DD} , V _{IN} = V _{SS} or V _{DD} , includes V _A SHDN=0 Pin Capacitance (All inputs/outputs) C _{IN} , C _{OUT} - 10 - pF V _{DD} = 5.0V, T _A = +25°C, f _C = 1 MHz Power Requirements Operating Voltage Range V _{DD} 2.7 - 5.5 V Supply Current, Active <t< td=""><td>Settling Time</td><td>t_S</td><td>_</td><td>18</td><td>l</td><td>μS</td><td>$V_A = V_{DD}, V_B = 0V, \pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF</td></t<>	Settling Time	t _S	_	18	l	μS	$V_A = V_{DD}, V_B = 0V, \pm 1\%$ Error Band, Transition from Code 00h to Code 80h, Output Load = 30 pF				
Digital Inputs/Outputs (CS, SCK, SI, SO) See Figure 2-12 for RS and SHDN pin operation. Schmitt Trigger High-Level Input Voltage V _{IH} 0.7V _{DD} — V Schmitt Trigger Low-Level Input Voltage V _{IL} — — 0.3V _{DD} V Hysteresis of Schmitt Trigger Inputs V _{HYS} — 0.05V _{DD} — U _{OL} = 2.1 mA, V _{DD} = 5V Low-Level Output Voltage V _{OL} — — V I _{OL} = 2.1 mA, V _{DD} = 5V High-Level Output Voltage V _{OH} V _{DD} - 0.5 — V I _{OH} = -400 μA, V _{DD} = 5V Input Leakage Current I _{LI} -1 — +1 μA CS = V _{DD} , V _{IN} = V _{SS} or V _{DD} , includes V _A SHDN=0 Pin Capacitance (All inputs/outputs) C _{IN} , C _{OUT} — 10 — pF V _{DD} = 5.0V, T _A = +25°C, f _C = 1 MHz Power Requirements Operating Voltage Range V _{DD} 2.7 — 5.5 V Supply Current, Active I _{DDA} — 340 500 μA V _{DD} = 5.5V, CS = V _{SS} , f _{SCK} = 10 MHz, SO = Open, Code FFh (Note 6)	Resistor Noise Voltage	e _{NWB}	_	29		nV/√Hz	V _A = Open, Code 80h, f =1 kHz				
Schmitt Trigger High-Level Input Voltage V_{IH} 0.7 V_{DD} — 0.3 V_{DD} V Schmitt Trigger Low-Level Input Voltage V_{IL} — 0.05 V_{DD} — 0.000 — 0.000 — 0.000 V_{DD} — 0.000	Crosstalk	C_{T}		-95		dB	$V_A = V_{DD}, V_B = 0V$ (Note 5)				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Digital Inputs/Outputs (CS, SCK, SI, SC		2-12 for R	S and SHI	ON pin ope	ration.					
Hysteresis of Schmitt Trigger Inputs V_{HYS} — $0.05V_{DD}$ — 0.40 V $I_{OL} = 2.1 \text{ mA}$, $V_{DD} = 5V$ Low-Level Output Voltage V_{OH} $V_{DD} - 0.5$ ——V $I_{OH} = -400 \mu A$, $V_{DD} = 5V$ High-Level Output Voltage V_{OH} $V_{DD} - 0.5$ ——V $I_{OH} = -400 \mu A$, $V_{DD} = 5V$ Input Leakage Current I_{LI} -1—+1 μA $\overline{CS} = V_{DD}$, $V_{IN} = V_{SS}$ or V_{DD} , includes V_A $\overline{SHDN} = 0$ Pin Capacitance (All inputs/outputs) C_{IN} , C_{OUT} —10—pF $V_{DD} = 5.0V$, $T_A = +25^{\circ}C$, $f_c = 1 \text{ MHz}$ Power RequirementsOperating Voltage Range V_{DD} 2.7—5.5VSupply Current, Active I_{DDA} —340500 μA $V_{DD} = 5.5V$, $\overline{CS} = V_{SS}$, $f_{SCK} = 10 \text{ MHz}$, $SO = Open$, Code FFh (Note 6)Supply Current, Static I_{DDS} —0.011 μA \overline{CS} , \overline{SHDN} , $\overline{RS} = V_{DD} = 5.5V$, SO = Open (Note 6)Power Supply SensitivityPSS—0.00150.0035%/% $V_{DD} = 4.5V - 5.5V$, $V_A = 4.5V$, Code 80h	Schmitt Trigger High-Level Input Voltage	V _{IH}	0.7V _{DD}	_		V					
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Schmitt Trigger Low-Level Input Voltage	V_{IL}	_	_	0.3V _{DD}	V					
High-Level Output Voltage V_{OH} V_{DD} - 0.5 $ V$ I_{OH} = -400 μ A, V_{DD} = 5V Input Leakage Current I_{LI} -1 $-$ +1 μ A \overline{CS} = V_{DD} , V_{IN} = V_{SS} or V_{DD} , includes V_A \overline{SHDN} =0 Pin Capacitance (All inputs/outputs) C_{IN} , C_{OUT} $-$ 10 $-$ pF V_{DD} = 5.0V, T_A = +25°C, T_C = 1 MHz Power Requirements Operating Voltage Range V_{DD} 2.7 $-$ 5.5 V Supply Current, Active I_{DDA} $-$ 340 500 μ A V_{DD} = 5.5V, \overline{CS} = V_{SS} , T_{SCK} = 10 MHz, T_{SO} = Open, Code FFh (Note 6) Supply Current, Static I_{DDS} $-$ 0.01 1 μ A \overline{CS} , \overline{SHDN} , \overline{RS} = V_{DD} = 5.5V, SO = Open (Note 6) Power Supply Sensitivity PSS $-$ 0.0015 0.0035 %/% V_{DD} = 4.5V - 5.5V, V_A = 4.5V, Code 80h	Hysteresis of Schmitt Trigger Inputs	V _{HYS}	_	0.05V _{DD}	_						
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Low-Level Output Voltage	V_{OL}	_	_	0.40	V	I _{OL} = 2.1 mA, V _{DD} = 5V				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	High-Level Output Voltage	V _{OH}	V _{DD} - 0.5			V					
Power Requirements Operating Voltage Range V _{DD} 2.7 — 5.5 V Supply Current, Active I _{DDA} — 340 500 μA V _{DD} = 5.5V, \overline{CS} = V _{SS} , f _{SCK} = 10 MHz, SO = Open, Code FFh (Note 6) Supply Current, Static I _{DDS} — 0.01 1 μA \overline{CS} , \overline{SHDN} , \overline{RS} = V _{DD} = 5.5V, SO = Open (Note 6) Power Supply Sensitivity PSS — 0.0015 0.0035 %/% V _{DD} = 4.5V - 5.5V, V _A = 4.5V, Code 80h	Input Leakage Current	I _{LI}	-1	_	+1	μA	$\overline{\text{CS}} = \text{V}_{\text{DD}}, \text{V}_{\text{IN}} = \text{V}_{\text{SS}} \text{ or V}_{\text{DD}}, \text{ includes V}_{\text{A}} \overline{\text{SHDN}} = 0$				
Power Requirements Operating Voltage Range V _{DD} 2.7 — 5.5 V Supply Current, Active I _{DDA} — 340 500 μA V _{DD} = 5.5V, \overline{CS} = V _{SS} , f _{SCK} = 10 MHz, SO = Open, Code FFh (Note 6) Supply Current, Static I _{DDS} — 0.01 1 μA \overline{CS} , \overline{SHDN} , \overline{RS} = V _{DD} = 5.5V, SO = Open (Note 6) Power Supply Sensitivity PSS — 0.0015 0.0035 %/% V _{DD} = 4.5V - 5.5V, V _A = 4.5V, Code 80h	Pin Capacitance (All inputs/outputs)	C _{IN} , C _{OUT}		10		pF	$V_{DD} = 5.0V$, $T_A = +25^{\circ}C$, $f_C = 1 \text{ MHz}$				
Supply Current, Active I_{DDA} — 340 500 μ A $V_{DD} = 5.5V$, $\overline{CS} = V_{SS}$, $f_{SCK} = 10$ MHz, $SO = Open$, Code FFh (Note 6) Supply Current, Static I_{DDS} — 0.01 1 μ A \overline{CS} , \overline{SHDN} , $\overline{RS} = V_{DD} = 5.5V$, SO = Open (Note 6) Power Supply Sensitivity PSS — 0.0015 0.0035 %/% $V_{DD} = 4.5V - 5.5V$, $V_{A} = 4.5V$, Code 80h	Power Requirements										
Supply Current, Active I_{DDA} — 340 500 μ A $V_{DD} = 5.5V$, $\overline{CS} = V_{SS}$, $f_{SCK} = 10$ MHz, $SO = Open$, Code FFh (Note 6) Supply Current, Static I_{DDS} — 0.01 1 μ A \overline{CS} , \overline{SHDN} , $\overline{RS} = V_{DD} = 5.5V$, SO = Open (Note 6) Power Supply Sensitivity PSS — 0.0015 0.0035 %/% $V_{DD} = 4.5V - 5.5V$, $V_{A} = 4.5V$, Code 80h	Operating Voltage Range	V_{DD}	2.7	_	5.5	V					
Power Supply Sensitivity PSS — 0.0015 0.0035 %/% V _{DD} = 4.5V - 5.5V, V _A = 4.5V, Code 80h	Supply Current, Active		_	340	500	μA	V_{DD} = 5.5V, \overline{CS} = V_{SS} , f_{SCK} = 10 MHz, SO = Open, Code FFh (Note 6)				
Power Supply Sensitivity PSS — 0.0015 0.0035 %/% V _{DD} = 4.5V - 5.5V, V _A = 4.5V, Code 80h	Supply Current, Static	I _{DDS}	_	0.01	1	μΑ	$\overline{\text{CS}}$, $\overline{\text{SHDN}}$, $\overline{\text{RS}}$ = V_{DD} = 5.5V, SO = Open (Note 6)				
			_	0.0015	0.0035	%/%	V _{DD} = 4.5V - 5.5V, V _A = 4.5V, Code 80h				
		PSS	_	0.0015	0.0035	%/%	V _{DD} = 2.7V - 3.3V, V _A = 2.7V, Code 80h				

Note

- 1:
- $V_{AB} = V_{DD}$, no connection on wiper. Rheostat position non-linearity R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from the ideal between successive tap positions. $I_W = 50 \mu A$ for $V_{DD} = 3V$ and $I_W = 400 \mu A$ for $V_{DD} = 5V$ for $10 k\Omega$ version. See Figure 2-26 for test circuit. INL and DNL are measured at V_W with the device configured in the voltage divider or potentiometer mode. $V_A = V_{DD}$ and $V_B = 0V$. DNL specification limits of ±1 LSB max are specified monotonic operating conditions. See Figure 2-25 for test circuit.
- Resistor terminals A,B and W have no restrictions on polarity with respect to each other. Full-scale and zero-scale error were measured
- Measured at V_W pin where the voltage on the adjacent V_W pin is swinging full-scale.
- Supply current is independent of current through the potentiometers.

Absolute Maximum Ratings †

V _{DD}	7.0V
All inputs and outputs w.r.t. V _{SS}	0.6V to V _{DD} +1.0V
Storage temperature	60°C to +150°C
Ambient temp. with power applied	60°C to +125°C
ESD protection on all pins	≥ 2 kV

† Notice: Stresses above those listed under "maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC TIMING CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, V _{DD} = +2.7V to 5.5V, T _A = -40°C to +85°C.											
Parameter	Sym	Min.	Тур.	Max.	Units	Conditions					
Clock Frequency	F _{CLK}	_	_	10	MHz	V _{DD} = 5V (Note 1)					
Clock High Time	t _{HI}	40	_	_	ns						
Clock Low Time	t _{LO}	40	_	_	ns						
CS Fall to First Rising CLK Edge	t _{CSSR}	40	_	_	ns						
Data Input Setup Time	t _{SU}	40	_	_	ns						
Data Input Hold Time	t _{HD}	10	_	_	ns						
SCK Fall to SO Valid Propagation Delay	t _{DO}		_	80	ns	C _L = 30 pF (Note 2)					
SCK Rise to CS Rise Hold Time	t _{CHS}	30	_	_	ns						
SCK Rise to CS Fall Delay	t _{CS0}	10	_	_	ns						
CS Rise to CLK Rise Hold	t _{CS1}	100	_	_	ns						
CS High Time	t _{CSH}	40	_	_	ns						
Reset Pulse Width	t _{RS}	150	_	_	ns	Note 2					
RS Rising to CS Falling Delay Time	t _{RSCS}	150	_	_	ns	Note 2					
CS rising to RS or SHDN falling delay time	t _{SE}	40	_	_	ns	Note 3					
CS low time	t _{CSL}	100	_	_	ns	Note 3					
Shutdown Pulse Width	t _{SH}	150	_	_	ns	Note 3					

Note
1: When using the device in the daisy-chain configuration, maximum clock frequency is determined by a combination of propagation delay time (t_{DO}) and data input setup time (t_{SU}). Max. clock frequency is therefore ~ 5.8 MHz based on SCK rise and fall times of 5 ns, t_{HI} = 40 ns, t_{DO} = 80 ns and t_{SU} = 40 ns.

^{2:} Applies only to the MCP42XXX devices.

^{3:} Applies only when using hardware pins to exit software shutdown mode, MCP42XXX only.

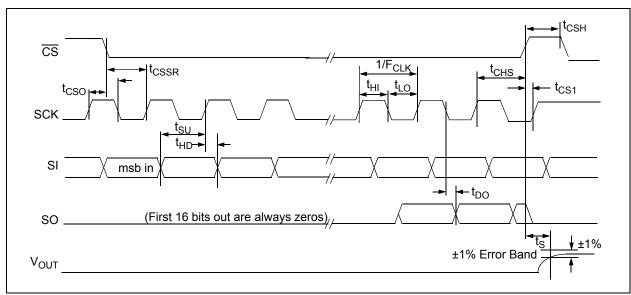


FIGURE 1-1: Detailed Serial interface Timing.

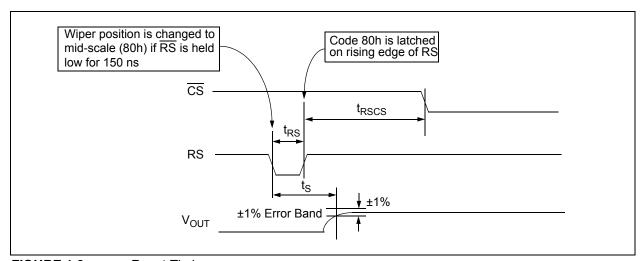


FIGURE 1-2: Reset Timing.

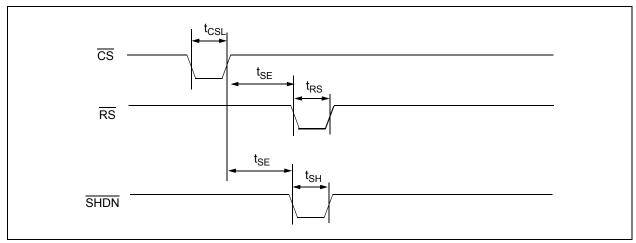


FIGURE 1-3: Software Shutdown Exit Timing.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

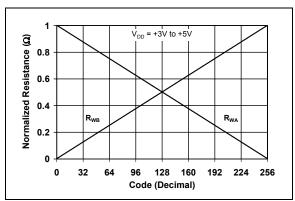


FIGURE 2-1: Normalized Wiper to End Terminal Resistance vs. Code.

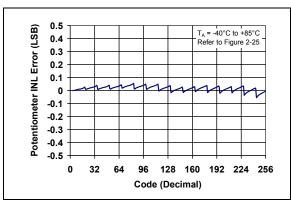


FIGURE 2-2: Potentiometer INL Error vs. Code.

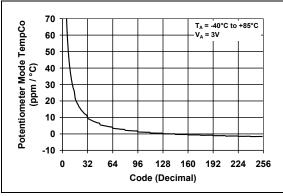


FIGURE 2-3: Potentiometer Mode Tempco vs. Code.

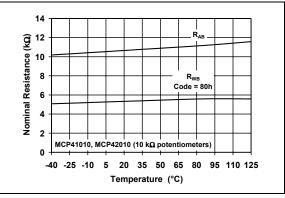


FIGURE 2-4: Nominal Resistance 10 $k\Omega$ vs. Temperature.

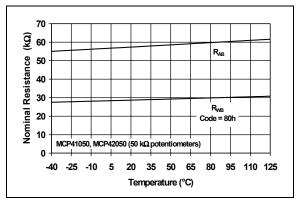


FIGURE 2-5: Nominal Resistance 50 $k\Omega$ vs. Temperature.

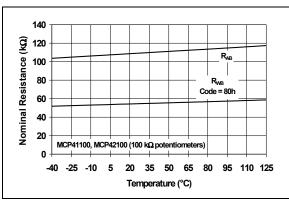


FIGURE 2-6: Nominal Resistance 100 $k\Omega$ vs. Temperature.

MCP41XXX/42XXX

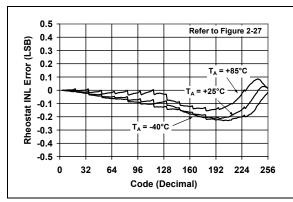


FIGURE 2-7: Rheostat INL Error vs. Code.

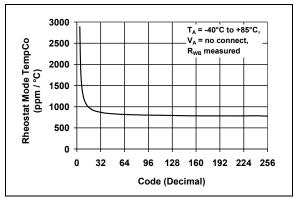


FIGURE 2-8: Rheostat Mode Tempco vs. Code.

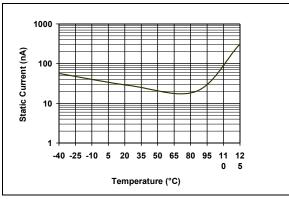


FIGURE 2-9: Static Current vs. Temperature.

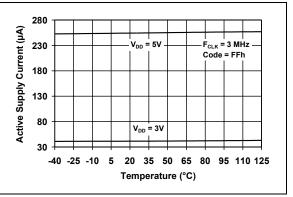


FIGURE 2-10: Active Supply Current vs. Temperature.

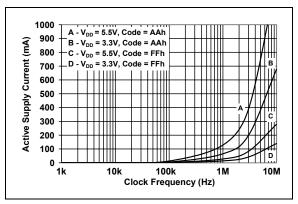


FIGURE 2-11: Active Supply Current vs. Clock Frequency.

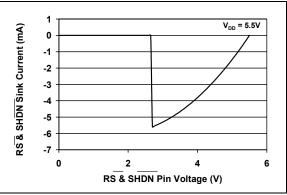


FIGURE 2-12: Reset & Shutdown Pins Current vs. Voltage.

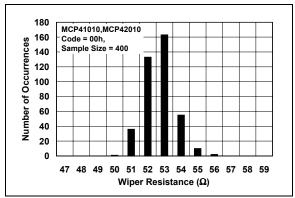


FIGURE 2-13: 10 kΩ Device Wiper Resistance Histogram.

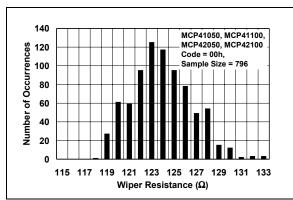


FIGURE 2-14: 50 kΩ, 100 kΩ Device Wiper Resistance Histogram.

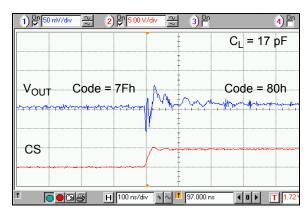


FIGURE 2-15: One Position Settling Time.

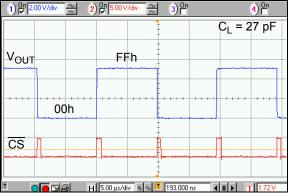


FIGURE 2-16: Full-Scale Settling Time.

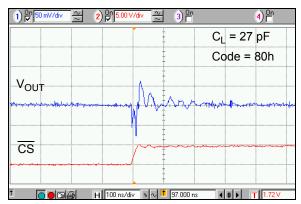


FIGURE 2-17: Digital Feed through vs. Time.

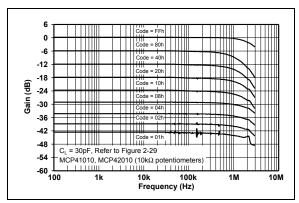


FIGURE 2-18: Gain vs. Frequency for $10 \text{ k}\Omega$ Potentiometer.

MCP41XXX/42XXX

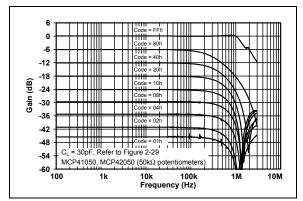


FIGURE 2-19: Gain vs. Frequency for $50k\Omega$ Potentiometer.

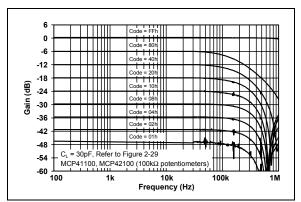


FIGURE 2-20: Gain vs. Frequency for 100kΩ Potentiometer.

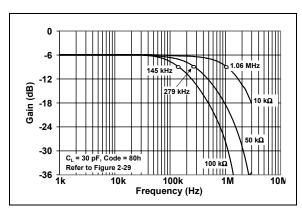


FIGURE 2-21: -3 dB Bandwidths.

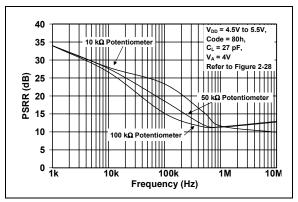


FIGURE 2-22: Power Supply Rejection Ratio vs. Frequency.

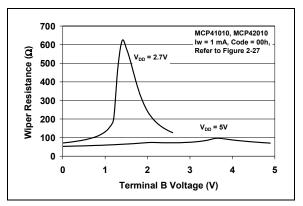


FIGURE 2-23: 10 k Ω Wiper Resistance vs. Voltage.

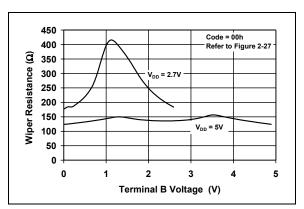


FIGURE 2-24: 50 kΩ & 100 kΩ Wiper Resistance vs. Voltage.

2.1 Parametric Test Circuits

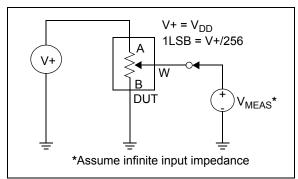


FIGURE 2-25: Potentiometer Divider Non-Linearity Error Test Circuit (DNL, INL).

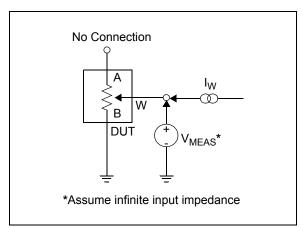


FIGURE 2-26: Resistor Position Non-Linearity Error Test Circuit (Rheostat operation DNL, INL).

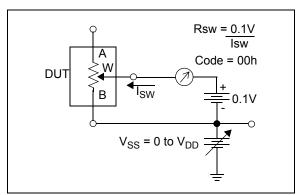


FIGURE 2-27: Wiper Resistance Test Circuit.

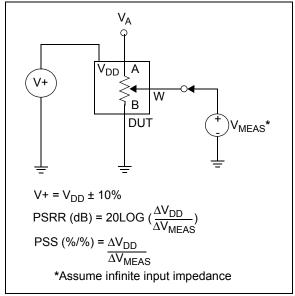


FIGURE 2-28: Power Supply Sensitivity Test Circuit (PSS, PSRR).

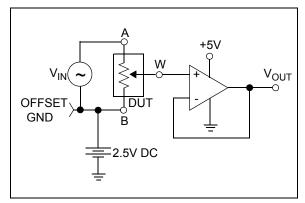


FIGURE 2-29: Gain vs. Frequency Test Circuit.

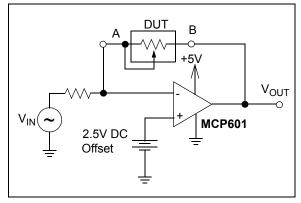


FIGURE 2-30: Capacitance Test Circuit.

3.0 PIN DESCRIPTIONS

3.1 PA0, PA1

Potentiometer Terminal A Connection.

3.2 PB0, PB1

Potentiometer Terminal B Connection.

3.3 PW0, PW1

Potentiometer Wiper Connection.

3.4 Chip Select (CS)

This is the SPI port chip select pin and is used to execute a new command after it has been loaded into the shift register. This pin has a Schmitt Trigger input.

3.5 Serial Clock (SCK)

This is the SPI port clock pin and is used to clock-in new register data. Data is clocked into the SI pin on the rising edge of the clock and out the SO pin on the falling edge of the clock. This pin is gated to the $\overline{\text{CS}}$ pin (i.e., the device will not draw any more current if the SCK pin is toggling when the $\overline{\text{CS}}$ pin is high). This pin has a Schmitt Trigger input.

3.6 Serial Data Input (SI)

This is the SPI port serial data input pin. The command and data bytes are clocked into the shift register using this pin. This pin is gated to the $\overline{\text{CS}}$ pin (i.e., the device will not draw any more current if the SI pin is toggling when the $\overline{\text{CS}}$ pin is high). This pin has a Schmitt Trigger input.

3.7 Serial Data Output (SO) (MCP42XXX devices only)

This is the SPI port serial data output pin used for daisy-chaining more than one device. Data is clocked out of the SO pin on the falling edge of clock. This is a push-pull output and **does not** go to a high-impedance state when $\overline{\text{CS}}$ is high. It will drive a logic-low when $\overline{\text{CS}}$ is high.

3.8 Reset (RS) (MCP42XXX devices only)

The Reset pin will set all potentiometers to mid-scale (Code 80h) if this pin is brought low for at least 150 ns. This pin should not be toggled low when the $\overline{\text{CS}}$ pin is low. It is possible to toggle this pin when the $\overline{\text{SHDN}}$ pin is low. In order to minimize power consumption, this pin has an active pull-up circuit. The performance of this circuit is shown in Figure 2-12. This pin will draw negligible current at logic level '0' and logic level '1'. Do not leave this pin floating.

3.9 Shutdown (SHDN) (MCP42XXX devices only)

The Shutdown pin has a Schmitt Trigger input. Pulling this pin low will put the device in a power-saving mode where A terminal is opened and the B and W terminals are connected for all potentiometers. This pin should not be toggled low when the \overline{CS} pin is low. In order to minimize power consumption, this pin has an active pull-up circuit. The performance of this circuit is shown in Figure 2-12. This pin will draw negligible current at logic level '0' and logic level '1'. Do not leave this pin floating.

TABLE 3-1: MCP41XXX Pins

Pin#	Name	Function				
1	CS	Chip Select				
2	SCK	Serial Clock				
3	SI	Serial Data Input				
4	V_{SS}	Ground				
5	PA0	Terminal A Connection For Pot 0				
6	PW0	Wiper Connection For Pot 0				
7	PB0	Terminal B Connection For Pot 0				
8	V_{DD}	Power				

TABLE 3-2: MCP42XXX Pins

Pin#	Name	Function
1	CS	Chip Select
2	SCK	Serial Clock
3	SI	Serial Data Input
4	V_{SS}	Ground
5	PB1	Terminal B Connection For Pot 1
6	PW1	Wiper Connection For Pot 1
7	PA1	Terminal A Connection For Pot 1
8	PA0	Terminal A Connection For Pot 0
9	PW0	Wiper Connection For Pot 0
10	PB0	Terminal B Connection For Pot 0
11	RS	Reset Input
12	SHDN	Shutdown Input
13	SO	Data Out for Daisy-Chaining
14	V_{DD}	Power

4.0 APPLICATIONS INFORMATION

The MCP41XXX/42XXX devices are 256 position single and dual digital potentiometers that can be used in place of standard mechanical pots. Resistance values of 10 k Ω , 50 k Ω and 100 k Ω are available. As shown in Figure 4-1, each potentiometer is made up of a variable resistor and an 8-bit (256 position) data register that determines the wiper position. There is a nominal wiper resistance of 52Ω for the 10 k Ω version, 125Ω for the 50 k Ω and 100 k Ω versions. For the dual devices, the channel-to-channel matching variation is less than 1%. The resistance between the wiper and either of the resistor endpoints varies linearly according to the value stored in the data register. Code 00h effectively connects the wiper to the B terminal. At

power-up, all data registers will automatically be loaded with the mid-scale value (80h). The serial interface provides the means for loading data into the shift register, which is then transferred to the data registers. The serial interface also provides the means to place individual potentiometers in the shutdown mode for maximum power savings. The $\overline{\text{SHDN}}$ pin can also be used to put all potentiometers in shutdown mode and the $\overline{\text{RS}}$ pin is provided to set all potentiometers to mid-scale (80h).

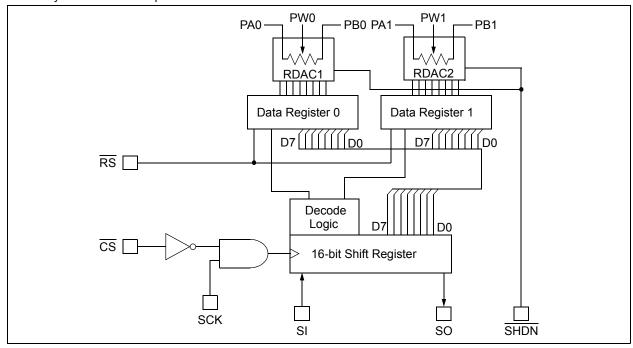
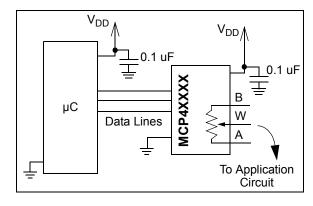


FIGURE 4-1: Block diagram showing the MCP42XXX dual digital potentiometer. Data register 0 and data register 1 are 8-bit registers allowing 256 positions for each wiper. Standard SPI pins are used with the addition of the Shutdown (SHDN) and Reset (RS) pins. As shown, reset affects the data register and wipers, bringing them to mid-scale. Shutdown disconnects the A terminal and connects the wiper to B, without changing the state of the data registers.



When laying out the circuit for your digital potentiometer, bypass capacitors should be used. These capacitors should be placed as close as possible to the device pin. A bypass capacitor value of 0.1 μF is recommended. Digital and analog traces should be separated as much as possible on the board, with no traces running underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high-frequency signals (such as clock lines) as far as possible from analog traces. Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board.

4.1 Modes of Operation

Digital potentiometer applications can be divided into two categories: rheostat mode and potentiometer, or voltage divider, mode.

4.1.1 RHEOSTAT MODE

In the rheostat mode, the potentiometer is used as a two-terminal resistive element. The unused terminal should be tied to the wiper, as shown in Figure 4-2. Note that reversing the polarity of the A and B terminals will not affect operation.

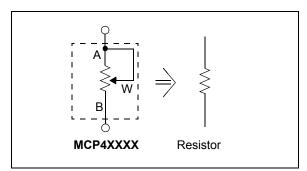


FIGURE 4-2: Two-terminal or rheostat configuration for the digital potentiometer. Acting as a resistive element in the circuit, resistance is controlled by changing the wiper setting.

Using the device in this mode allows control of the total resistance between the two nodes. The total measured resistance would be the least at code 00h, where the wiper is tied to the B terminal. The resistance at this code is equal to the wiper resistance, typically 52Ω for the $10~k\Omega$ MCP4X010 devices, 125Ω for the $50~k\Omega$ (MCP4X050), and $100~k\Omega$ (MCP4X100) devices. For the $10~k\Omega$ device, the LSB size would be 39.0625Ω (assuming $10~k\Omega$ total resistance). The resistance would then increase with this LSB size until the total measured resistance at code FFh would be 9985.94Ω . The wiper will never directly connect to the A terminal of the resistor stack.

In the 00h state, the total resistance is the wiper resistance. To avoid damage to the internal wiper circuitry in this configuration, care should be taken to ensure the current flow never exceeds 1 mA.

For dual devices, the variation of channel-to-channel matching of the total resistance from A to B is less than 1%. The device-to-device matching, however, can vary up to 30%. In the rheostat mode, the resistance has a positive temperature coefficient. The change in wiper-to-end terminal resistance over temperature is shown in Figure 2-8. The most variation over temperature will occur in the first 6% of codes (code 00h to 0Fh) due to the wiper resistance coefficient affecting the total resistance. The remaining codes are dominated by the total resistance tempco R_{AB} , typically 800 ppm/°C.

4.1.2 POTENTIOMETER MODE

In the potentiometer mode, all three terminals of the device are tied to different nodes in the circuit. This allows the potentiometer to output a voltage proportional to the input voltage. This mode is sometimes called voltage divider mode. The potentiometer is used to provide a variable voltage by adjusting the wiper position between the two endpoints as shown in Figure 4-3. Note that reversing the polarity of the A and B terminals will not affect operation.

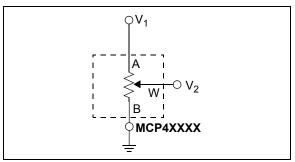


FIGURE 4-3: Three terminal or voltage divider mode.

In this configuration, the ratio of the internal resistance defines the temperature coefficient of the device. The resistor matching of the R_{WB} resistor to the R_{AB} resistor performs with a typical temperature coefficient of 1 ppm/°C (measured at code 80h). At lower codes, the wiper resistance temperature coefficient will dominate. Figure 2-3 shows the effect of the wiper. Above the lower codes, this figure shows that 70% of the states will typically have a temperature coefficient of less than 5 ppm/°C. 30% of the states will typically have a ppm/°C of less than 1.

4.2 Typical Applications

4.2.1 PROGRAMMABLE SINGLE-ENDED AMPLIFIERS

Potentiometers are often used to adjust system reference levels or gain. Programmable gain circuits using digital potentiometers can be realized in a number of different ways. An example of a single-supply, inverting gain amplifier is shown in Figure 4-4. Due to the high input impedance of the amplifier, the wiper resistance is not included in the transfer function. For a single-supply, non-inverting gain configuration, the circuit in Figure 4-5 can be used.

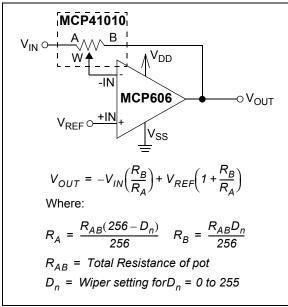


FIGURE 4-4: Single-supply, programmable, inverting gain amplifier using a digital potentiometer.

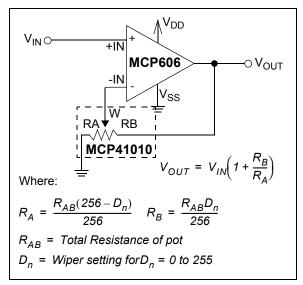


FIGURE 4-5: Single-supply, programmable, non-inverting gain amplifier.

In order for these circuits to work properly, care must be taken in a few areas. For linear operation, the analog input and output signals must be in the range of V_{SS} to V_{DD} for the potentiometer and input and output rails of the op-amp. The circuit in Figure 4-4 requires a virtual ground or reference input to the non-inverting input of the amplifier. Refer to Application Note 682, "Using Single-Supply Operational Amplifiers in Embedded Systems" (DS00682), for more details. At power-up or reset (RS), the resistance is set to mid-scale, with R_A and R_B matching. Based on the transfer function for the circuit, the gain is -1 V/V. As the code is increased and the wiper moves towards the A terminal, the gain increases. Conversely, when the wiper is moved towards the B terminal, the gain decreases. Figure 4-6 shows this relationship. Notice the pseudo-logarithmic gain around decimal code 128. As the wiper approaches either terminal, the step size in the gain calculation increases dramatically. Due to the mismatched ratio of RA and RB at the extreme high and low codes, small increments in wiper position can dramatically affect the gain. As shown in Figure 4-3, recommended gains lie between 0.1 and 10 V/V.

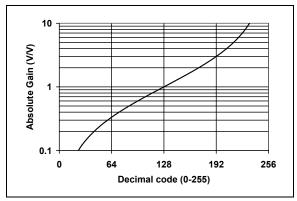


FIGURE 4-6: Gain vs. Code for inverting and differential amplifier circuits.

4.2.2 PROGRAMMABLE DIFFERENTIAL AMPLIFIER

An example of a differential input amplifier using digital potentiometers is shown in Figure 4-7. For the transfer function to hold, both pots must be programmed to the same code. The resistor-matching from channel-to-channel within a dual device can be used as an advantage in this circuit. This circuit will also show stable operation over temperature due to the low potentiometer temperature coefficient. Figure 4-6 also shows the relationship between gain and code for this circuit. As the wiper approaches either terminal, the step size in the gain calculation increases dramatically. This circuit is recommended for gains between 0.1 and 10 V/V.

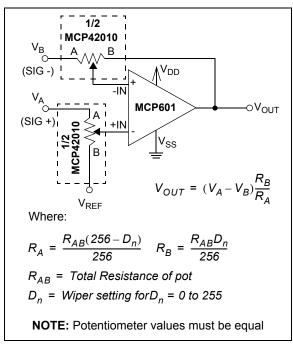


FIGURE 4-7: Single Supply programmable differential amplifier using digital potentiometers.

4.2.3 PROGRAMMABLE OFFSET TRIM

For applications requiring only a programmable voltage reference, the circuit in Figure 4-8 can be used. This circuit shows the device used in the potentiometer mode along with two resistors and a buffered output. This creates a circuit with a linear relationship between voltage-out and programmed code. Resistors R_1 and R_2 can be used to increase or decrease the output voltage step size. The potentiometer in this mode is stable over temperature. The operation of this circuit over temperature is shown in Figure 2-3. The worst performance over temperature will occur at the lower codes due to the dominating wiper resistance. R_1 and R_2 can also be used to affect the boundary voltages, thereby eliminating the use of these lower codes.

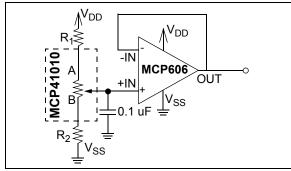


FIGURE 4-8: By changing the values of R_1 and R_2 , the voltage output resolution of this programmable voltage reference circuit is affected.

4.3 Calculating Resistances

When programming the digital potentiometer settings, the following equations can be used to calculate the resistances. Programming code 00h effectively brings the wiper to the B terminal, leaving only the wiper resistance. Programming higher codes will bring the wiper closer to the A terminal of the potentiometer. The equations in Figure 4-9 can be used to calculate the terminal resistances. Figure 4-10 shows an example calculation using a 10 k Ω potentiometer.

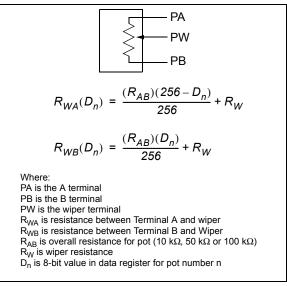


FIGURE 4-9: Potentiometer resistances are a function of code. It should be noted that, when using these equations for most feedback amplifier circuits (see Figure 4-4 and Figure 4-5), the wiper resistance can be omitted due to the high impedance input of the amplifier.

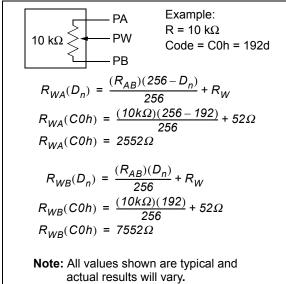


FIGURE 4-10: Example Resistance calculations.

5.0 SERIAL INTERFACE

Communications from the controller to the MCP41XXX/42XXX digital potentiometers is accomplished using the SPI serial interface. This interface allows three commands:

- Write a new value to the potentiometer data register(s).
- 2. Cause a channel to enter low power shutdown mode.
- 3. NOP (No Operation) command.

Executing any command is accomplished by setting $\overline{\text{CS}}$ low and then clocking-in a command byte followed by a data byte into the $\underline{16}$ -bit shift register. The command is executed when $\overline{\text{CS}}$ is raised. Data is clocked-in on the rising edge of clock and out the SO pin on the falling edge of the clock (see Figure 5-1). The device will track the number of clocks (rising edges) while $\overline{\text{CS}}$ is low and will abort all commands if the number of clocks is not a multiple of 16.

5.1 Command Byte

The first byte sent is always the command byte, followed by the data byte. The command byte contains two command select bits and two potentiometer select bits. Unused bits are 'don't care' bits. The command select bits are summarized in Figure 5-2. The command select bits C1 and C0 (bits 4:5) of the command byte determine which command will be executed. If the command bits are both 0's or 1's, then a NOP command will be executed once all 16 bits have been loaded. This command is useful when using the daisychain configuration. When the command bits are 0,1, a write command will be executed with the 8 bits sent in the data byte. The data will be written to the potentiometer(s) determined by the potentiometer select bits. If the command bits are 1,0, then a shutdown command will be executed on the potentiometers determined by the potentiometer select bits.

For the MCP42XXX devices, the potentiometer select bits P1 and P0 (bits 0:1) determine which potentiometers are to be acted upon by the command. A corresponding '1' in the position signifies that the command for that potentiometer will get executed, while a '0' signifies that the command will not effect that potentiometer (see Figure 5-2).

5.2 Writing Data Into Data Registers

When new data is written into one or more of the potentiometer data registers, the write command is followed by the data byte for the new value. The command select bits C1, C0 are set to 0,1. The potentiometer selection bits P1 and P0 allow new values to be written to potentiometer 0, potentiometer 1 (or both) with a single command. A '1' for either P1 or P0 will cause the data to be written to the respective data register and a '0' for P1 or P0 will cause no change. See Figure 5-2 for the command format summary.

5.3 Using The Shutdown Command

The shutdown command allows the user to put the application circuit into a power-saving mode. In this mode, the A terminal is open-circuited and the B and W terminals are shorted together. The command select bits C1, C0 are set to 1,0. The potentiometer selection bits P1 and P0 allow each potentiometer to be shutdown independently. If either P1 or P0 are high, the respective potentiometer will enter shutdown mode. A '0' for P1 or P0 will have no effect. The eight data bits following the command byte still need to be transmitted for the shutdown command, but they are 'don't care' bits. See Figure 5-2 for command format summary. Once a particular potentiometer has entered the shutdown mode, it will remain in this mode until:

• A new value is written to the potentiometer data register, provided that the SHDN pin is high. The device will remain in the shutdown mode until the rising edge of the CS is detected, at which time the device will come out of shutdown mode and the new value will be written to the data register(s). If the SHDN pin is low when the new value is received, the registers will still be set to the new value, but the device will remain in shutdown mode. This scenario assumes that a valid command was received, the command will be ignored and the device will remain in the shutdown mode.

It is also possible to use the hardware shutdown pin and reset pin to remove a device from software shutdown. To do this, a low pulse on the chip select line must first be sent. For multiple devices, sharing a single SHDN or RESET line allows you to pick an individual device on that chain to remove from software shutdown mode. See Figure 1-3 for timing. With a preceding chip select pulse, either of these situations will also remove a device from software shutdown:

- A falling edge is seen on the RS pin and held low for at least 150 ns, provided that the SHDN pin is high. If the SHDN pin is low, the registers will still be set to mid-scale, but the device will remain in shutdown mode. This condition assumes that CS is high, as bringing the RS pin low while CS is low is an invalid state and results are indeterminate.
- A rising edge on the SHDN pin is seen after being low for at least 100 ns, provided that the CS pin is high. Toggling the SHDN pin low while CS is low is an invalid state and results are indeterminate.
- · The device is powered-down and back up.

Note: The hardware SHDN pin will always put the device in shutdown regardless of whether a potentiometer has already been put in the shutdown mode using the software command.

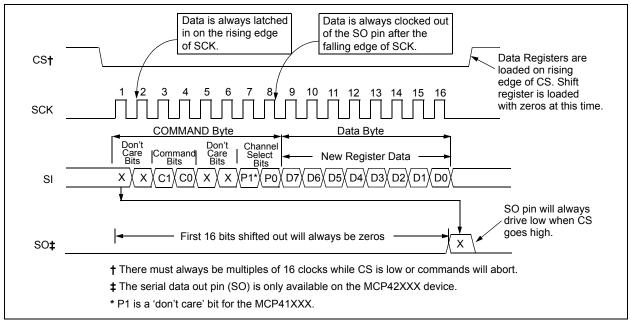


FIGURE 5-1: Timing Diagram for Writing Instructions or Data to a Digital Potentiometer.

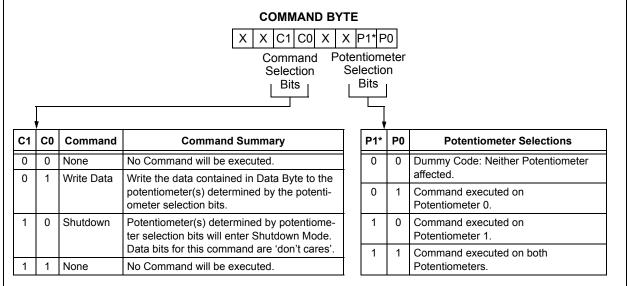


FIGURE 5-2: Command Byte Format.

5.4 Daisy-Chain Configuration

Multiple MCP42XXX devices can be connected in a daisy-chain configuration, as shown in Figure 5-4, by connecting the SO pin from one device to the SI pin on the next device. The data on the SO pin is the output of the 16-bit shift register. The daisy-chain configuration allows the system designer to communicate with several devices without using a separate CS line for each device. The example shows a daisy-chain configuration with three devices, although any number of devices (with or without the same resistor values) can be configured this way. While it is not possible to use a MCP41XXX at the beginning or middle of a daisy-chain (because it does not provide the serial data out (SO) pin), it is possible to use the device at the end of a chain. As shown in the timing diagram in Figure 5-3, data will be clocked-out of the SO pin on the falling edge of the clock. The SO pin has a CMOS push-pull output and will drive low when $\overline{\text{CS}}$ goes high. SO will **not** go to a high-impedance state when \overline{CS} is held high.

When using the daisy-chain configuration, the maximum clock speed possible is reduced to ~5.8 MHz, because of the propagation delay of the data coming out of the SO pin.

When using the daisy-chain configuration, keep in mind that the shift register of each device is automatically loaded with zeros whenever a command is executed (CS = high). Because of this, the first 16 bits that come out of the SO pin once the CS line goes low will always be zeros. This means that when the first command is being loaded into a device, it will always shift a NOP command into the next device on the chain because the command bits (and all the other bits) will be zeros. This feature makes it necessary only to send command and data bytes to the device farthest down the chain that needs a new command. For example, if there were three devices on the chain and it was desired to send a command to the device in the middle, only 32 bytes of data need to be transmitted. The last device on the chain will have a NOP loaded from the previous device so no registers will be affected when the CS pin is raised to execute the command. The user must always ensure that multiples of 16 clocks are always provided (while CS is low), as all commands will abort if the number of clocks provided is not a multiple of 16.

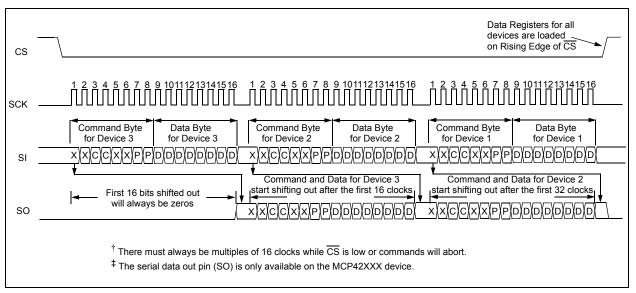


FIGURE 5-3: Timing Diagram for Daisy-Chain Configuration.

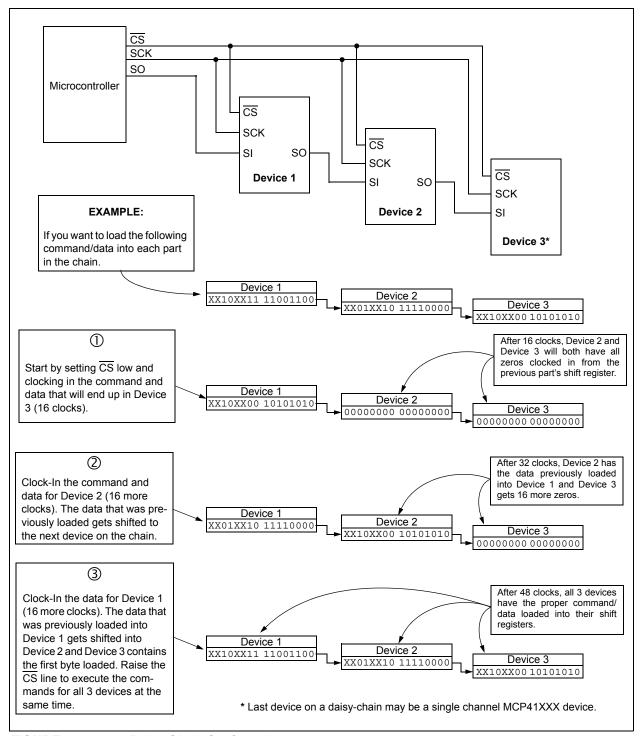


FIGURE 5-4: Daisy-Chain Configuration.

5.5 Reset (RS) Pin Operation

The Reset pin (\overline{RS}) will automatically set all potentiometer data latches to mid-scale (Code 80h) when pulled low (provided that the pin is held low at least 150 ns and \overline{CS} is high). The reset will execute regardless of the position of the SCK, \overline{SHDN} and SI pins. It is possible to toggle \overline{RS} low and back high while \overline{SHDN} is low. In this case, the potentiometer registers will reset to mid-scale, but the potentiometer will remain in shutdown mode until the \overline{SHDN} pin is raised.

Note: Bringing the RS pin low while the CS pin is low constitutes an invalid operating state and will result in indeterminate results when RS and/or CS are brought high.

5.6 Shutdown (SHDN) Pin Operation

When held low, the shutdown pin causes the application circuit to go into a power-saving mode by open-circuiting the A terminal and shorting the B and W terminals for all potentiometers. Data register contents are not affected by entering shutdown mode (i.e., when the SHDN pin is raised, the data register contents are the same as before the shutdown mode was entered).

While in shutdown mode, it is still possible to clock in new values for the data registers, as well as toggling the $\overline{\text{RS}}$ pin to cause all data registers to go to mid-scale. The new values will take affect when the $\overline{\text{SHDN}}$ pin is raised.

If the device is powered-up with the \overline{SHDN} pin held low, it will power-up in the shutdown mode with the data registers set to mid-scale.

Note: Bringing the SHDN pin low while the CS pin is low constitutes an invalid operating state and will result in indeterminate results when SHDN and/or CS are brought high.

5.7 Power-up Considerations

When the device is powered on, the data registers will be set to mid-scale (80h). A power-on reset circuit is utilized to ensure that the device powers up in this known state.

TABLE 5-1: TRUTH TABLE FOR LOGIC INPUTS

SCK	cs	RS	SHDN	Action
X	Ø	Н	Н	Communication is initiated with device. Device comes out of standby mode.
L	L	Н	Н	No action. Device is waiting for data to be clocked into shift register or $\overline{\text{CS}}$ to go high to execute command.
-	┙	Ħ	Х	Shift one bit into shift register. The shift register can be loaded while the SHDN pin is low.
Ø	L	Ħ	Х	Shift one bit out of shift register on the SO pin. The SO pin is active while the SHDN pin is low.
X		I	I	Based on command bits, either load data from shift register into data latches or execute shutdown command. Neither command executed unless multiples of 16 clocks have been entered while $\overline{\text{CS}}$ is low. SO pin goes to a logic low.
Χ	Н	Н	Н	Static Operation.
Х	Н	Ø	Н	All data registers set and latched to code 80h.
X	Η	Ø	L	All data registers set and latched to code 80h. Device is in hardware shutdown mode and will remain in this mode.
X	Н	Н	Ø	All potentiometers put into hardware shutdown mode; terminal A is open and W is shorted to B.
X	Н	Н	-	All potentiometers exit hardware shutdown mode. Potentiometers will also exit software shutdown mode if this rising edge occurs after a low pulse on CS. Contents of data latches are restored.

5.8 Using the MCP41XXX/42XXX in SPI Mode 1,1

It is possible to operate the devices in SPI modes 0,0 and 1,1. The only difference between these two modes is that, when using mode 1,1, the clock idles in the high state, while in mode 0,0, the clock idles in the low state. In both modes, data is clocked into the devices on the rising edge of SCK and data is clocked out the SO pin once the falling edge of SCK. Operations using mode 0,0 are shown in Figure 5-1. The example in Figure 5-5 shows mode 1,1.

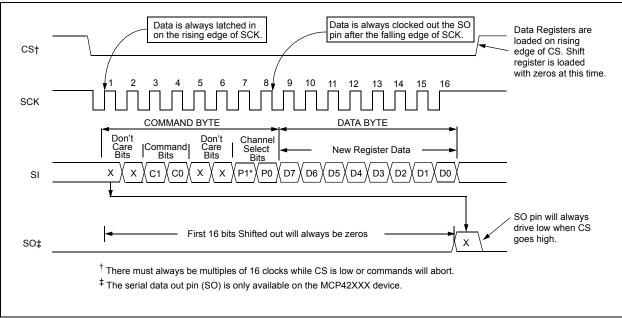
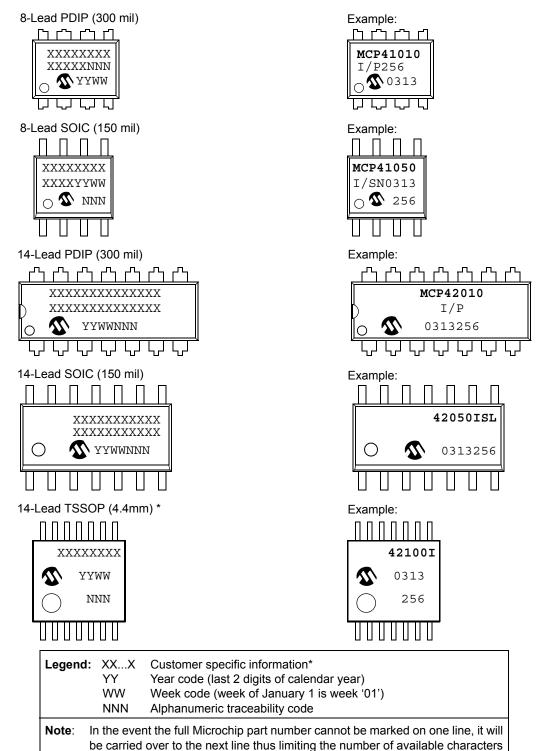


FIGURE 5-5: Timing Diagram for SPI Mode 1,1 Operation.

6.0 PACKAGING INFORMATION

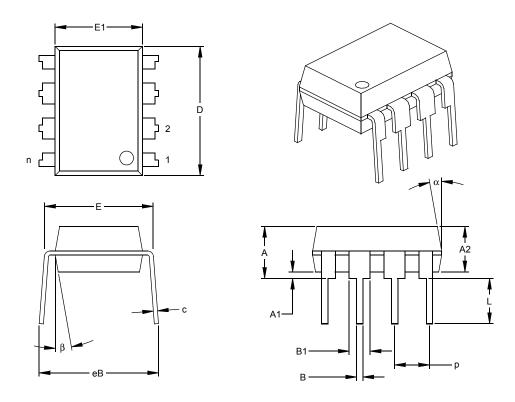
6.1 Package Marking Information



^{*} Standard marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code.

for customer specific information.

8-Lead Plastic Dual In-line (P) - 300 mil (PDIP)



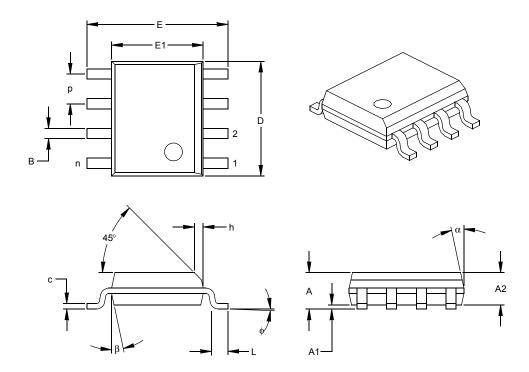
	Units		INCHES*		MILLIMETERS			
Dimension	MIN	NOM	MAX	MIN	NOM	MAX		
Number of Pins	n		8			8		
Pitch	р		.100			2.54		
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32	
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	Е	.300	.313	.325	7.62	7.94	8.26	
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60	
Overall Length	D	.360	.373	.385	9.14	9.46	9.78	
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43	
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78	
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56	
Overall Row Spacing §	eВ	.310	.370	.430	7.87	9.40	10.92	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MS-001 Drawing No. C04-018

^{*} Controlling Parameter § Significant Characteristic

8-Lead Plastic Small Outline (SN) - Narrow, 150 mil (SOIC)



	Units		INCHES*		MILLIMETERS		
Dimensio	n Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.050			1.27	
Overall Height	Α	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	Е	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	ф	0	4	8	0	4	8
Lead Thickness	С	.008	.009	.010	0.20	0.23	0.25
Lead Width	В	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

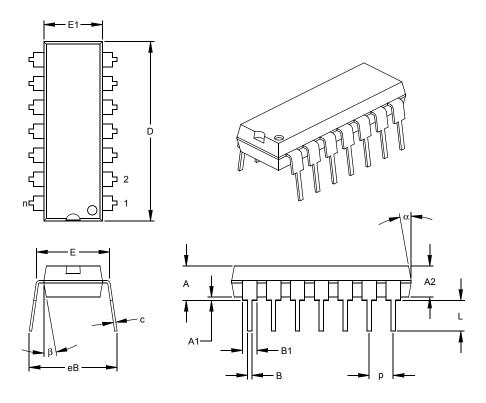
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

^{*} Controlling Parameter § Significant Characteristic

14-Lead Plastic Dual In-line (P) - 300 mil (PDIP)



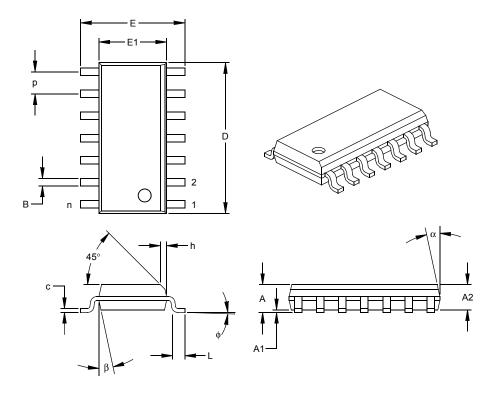
	Units		INCHES*		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	Е	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eВ	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

^{*} Controlling Parameter § Significant Characteristic

14-Lead Plastic Small Outline (SL) - Narrow, 150 mil (SOIC)



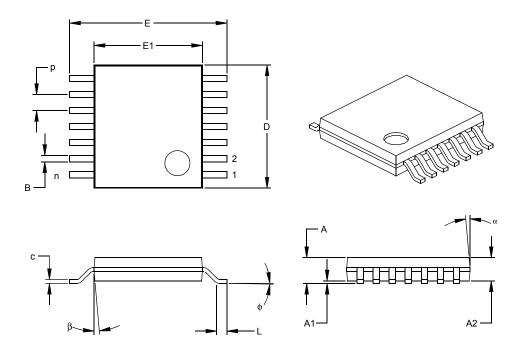
	Units		INCHES*		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		14			14		
Pitch	р		.050			1.27		
Overall Height	Α	.053	.061	.069	1.35	1.55	1.75	
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55	
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25	
Overall Width	Е	.228	.236	.244	5.79	5.99	6.20	
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99	
Overall Length	D	.337	.342	.347	8.56	8.69	8.81	
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51	
Foot Length	L	.016	.033	.050	0.41	0.84	1.27	
Foot Angle	ф	0	4	8	0	4	8	
Lead Thickness	С	.008	.009	.010	0.20	0.23	0.25	
Lead Width	В	.014	.017	.020	0.36	0.42	0.51	
Mold Draft Angle Top	α	0	12	15	0	12	15	
Mold Draft Angle Bottom	β	0	12	15	0	12	15	

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

^{*} Controlling Parameter § Significant Characteristic

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



	Units	INCHES			MILLIMETERS*		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	р		.026			0.65	
Overall Height	Α			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	Е	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ф	0	4	8	0	4	8
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20
Lead Width	В	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.005" (0.127mm) per side. JEDEC Equivalent: MO-153 Drawing No. C04-087

^{*} Controlling Parameter § Significant Characteristic

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u> </u>			Examples:			
Device 1	Temperature Range	 Package	a) b) c)	MCP41010-I/SN: MCP41010-E/P: MCP41010T-I/SN: MCP41050-E/SN:	8LD SOIC pkg.		
Device:	MCP41010T: MCP41050T: MCP411050T: MCP41100T: MCP41100T: MCP42010T: MCP42010T: MCP42050T: MCP42050T: MCP42100:	Single Digital Potentiometer (10 k Ω) Single Digital Potentiometer (10 k Ω) (Tape and Reel) Single Digital Potentiometer (50 k Ω) (Tape and Reel) Single Digital Potentiometer (50 k Ω) Single Digital Potentiometer (100 k Ω) (Tape and Reel) Single Digital Potentiometer (100 k Ω) (Tape and Reel) Single Digital Potentiometer (100 k Ω) Dual Digital Potentiometer (10 k Ω) Dual Digital Potentiometer (10 k Ω) (Tape and Reel) Dual Digital Potentiometer (50 k Ω) Dual Digital Potentiometer (50 k Ω) (Tape and Reel) Dual Digital Potentiometer (100 k Ω) Dual Digital Potentiometer (100 k Ω) Dual Digital Potentiometer (100 k Ω) (Tape and Reel)	e) f) g) h) i) a) b) c) d) e) f) g) h) h) c) c) d) h) c) c) d) h) c) c) d)	MCP41050-I/P: MCP41050-E/SN: MCP41100-I/SN: MCP41100-E/P: MCP42010-E/P: MCP42010-I/SL: MCP42010-E/ST: MCP42010-I/ST: MCP42050-E/P: MCP42050-I/SL: MCP42050-I/SL: MCP42050-I/SL: MCP42050-I/ST:	E-Temp., 14LD PDIP pkg. I-Temp., 14LD SOIC pkg. E-Temp., 14LD TSSOP pkg. Tape and Reel, I-Temp., 14LD TSSOP pkg. E-Temp., 14LD PDIP pkg. Tape and Reel, I-Temp., 14LD SOIC pkg. E-Temp., 14LD SOIC pkg. I-Temp., 14LD TSSOP pkg.		
Temperature Range:		0°C to +85°C 0°C to +125°C	j)	MCP42050T-I/SL: MCP42050T-I/ST:	Tape and Reel, I-Temp., 14LD SOIC pkg. Tape and Reel, I-Temp., 14LD TSSOP pkg.		
Package:	P = SN = SL = ST =	Plastic DIP (300 mil Body), 8-lead, 14-lead Plastic SOIC (150 mil Body), 8-lead Plastic SOIC (150 mil Body), 14-lead TSSOP (4.4mm Body), 14-lead	k)) m) n) o)	MCP42100-E/P: MCP42100-I/SL: MCP42100-E/ST: MCP42100T-I/SL: MCP42100T-I/ST:	E-Temp., 14LD PDIP pkg. I-Temp., 14LD SOIC pkg. E-Temp., 14LD TSSOP pkg. Tape and Reel, I-Temp., 14LD SOIC pkg. Tape and Reel, I-Temp., 14LD TSSOP pkg.		

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

- 1. Your local Microchip sales office
- 2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
- 3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

MCP41XXX/42XXX

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, MPLAB, PIC, PICmicro, PICSTART, PRO MATE and PowerSmart are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, microID, MXDEV, MXLAB, PICMASTER, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Accuron, Application Maestro, dsPICDEM, dsPICDEM.net, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICC, PICkit, PICDEM, PICDEM.net, PowerCal, PowerInfo, PowerMate, PowerTool, rfLAB, rfPIC, Select Mode, SmartSensor, SmartShunt, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2003, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.



Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200

Fax: 480-792-7277 Technical Support: 480-792-7627 Web Address: http://www.microchip.com

Atlanta

3780 Mansell Road, Suite 130 Alpharetta, GA 30022 Tel: 770-640-0034 Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120 Westford, MA 01886 Tel: 978-692-3848 Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180 Itasca, IL 60143 Tel: 630-285-0071 Fax: 630-285-0075

4570 Westgrove Drive, Suite 160 Addison, TX 75001 Tel: 972-818-7423 Fax: 972-818-2924

Detroit

Tri-Atria Office Building 32255 Northwestern Highway, Suite 190 Farmington Hills, MI 48334

Tel: 248-538-2250 Fax: 248-538-2260

Kokomo

2767 S. Albright Road Kokomo, IN 46902 Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090 Irvine, CA 92612 Tel: 949-263-1888 Fax: 949-263-1338

Phoenix

2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7966 Fax: 480-792-4338

San Jose

2107 North First Street, Suite 590 San Jose, CA 95131 Tel: 408-436-7950

Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108 Mississauga, Ontario L4V 1X5, Canada

Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Suite 22, 41 Rawson Street Epping 2121, NSW Australia Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Unit 915

Bei Hai Wan Tai Bldg. No. 6 Chaoyangmen Beidajie Beijing, 100027, No. China Tel: 86-10-85282100 Fax: 86-10-85282104 China - Chengdu

Rm. 2401-2402, 24th Floor, Ming Xing Financial Tower No. 88 TIDU Street Chengdu 610016, China Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou

Unit 28F. World Trade Plaza No. 71 Wusi Road Fuzhou 350001, China Tel: 86-591-7503506 Fax: 86-591-7503521

China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza 223 Hing Fong Road Kwai Fong, N.T., Hong Kong

Tel: 852-2401-1200 Fax: 852-2401-3431

China - Shanghai Room 701, Bldg. B Far East International Plaza No. 317 Xian Xia Road Shanghai, 200051 Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza No. 5022 Binhe Road, Futian District Shenzhen 518033, China

Tel: 86-755-82901380 Fax: 86-755-8295-1393

China - Shunde

Room 401, Hongjian Building No. 2 Fengxiangnan Road, Ronggui Town Shunde City, Guangdong 528303, China Tel: 86-765-8395507 Fax: 86-765-8395571

China - Qingdao

Rm. B505A, Fullhope Plaza, No. 12 Hong Kong Central Rd. Qinqdao 266071. China Tel: 86-532-5027355 Fax: 86-532-5027205

India

Divyasree Chambers 1 Floor, Wing A (A3/A4) No. 11, O'Shaugnessey Road Bangalore, 560 025, India Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Benex S-1 6F 3-18-20, Shinyokohama Kohoku-Ku, Yokohama-shi Kanagawa, 222-0033, Japan Tel: 81-45-471- 6166 Fax: 81-45-471-6122 Korea

168-1, Youngbo Bldg. 3 Floor Samsung-Dong, Kangnam-Ku Seoul, Korea 135-882 Tel: 82-2-554-7200 Fax: 82-2-558-5932 or

82-2-558-5934

Singapore 200 Middle Road #07-02 Prime Centre Singapore, 188980

Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Kaohsiung Branch 30F - 1 No. 8 Min Chuan 2nd Road Kaohsiung 806, Taiwan Tel: 886-7-536-4818 Fax: 886-7-536-4803

Taiwan

Taiwan Branch 11F-3, No. 207 Tung Hua North Road Taipei, 105, Taiwan

Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria

Durisolstrasse 2 A-4600 Wels Austria

Tel: 43-7242-2244-399 Fax: 43-7242-2244-393

Denmark

Regus Business Centre Lautrup hoj 1-3 Ballerup DK-2750 Denmark

Tel: 45-4420-9895 Fax: 45-4420-9910

France

Parc d'Activite du Moulin de Massy 43 Rue du Saule Trapu Batiment A - Ier Etage 91300 Massy, France Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Steinheilstrasse 10 D-85737 Ismaning, Germany Tel: 49-89-627-144-0 Fax: 49-89-627-144-44

Italy

Via Quasimodo, 12 20025 Legnano (MI) Milan, Italy Tel: 39-0331-742611 Fax: 39-0331-466781

Netherlands

P. A. De Biesbosch 14 NL-5152 SC Drunen, Netherlands Tel: 31-416-690399

Fax: 31-416-690340 **United Kingdom**

505 Eskdale Road Winnersh Triangle

Wokingham Berkshire, England RG41 5TU Tel: 44-118-921-5869 Fax: 44-118-921-5820

07/28/03

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Microchip:

MCP42100-I/SL MCP42100-I/P MCP42100-I/ST MCP42050-I/SL MCP42050-I/ST MCP42010-I/ST MCP42010-I/ST MCP42010-I/ST MCP42010-I/ST MCP42010-I/ST MCP42010-I/ST MCP42010-I/ST MCP42010-I/ST MCP42050-E/P MCP41100-E/SN MCP41050-E/SN MCP41010-E/SN MCP41010-E/P MCP42100T-E/ST MCP42010T-E/SL MCP41050T-I/SN MCP4100T-I/SN MCP42010T-E/ST MCP42050T-E/SL MCP41010T-I/SN MCP42050T-E/ST MCP42050T-E/ST MCP42050T-I/SL MCP42050T-I/SL MCP42050T-I/SL MCP42010T-I/SL MCP42010T-I/SL MCP42010T-I/SL MCP42010T-I/SL MCP42010T-I/SL MCP42010T-I/SL MCP42010-E/ST MCP42010-E/SL MCP42010-E/ST MCP42050-E/ST MCP42010-E/SL MCP42010-I/SN MCP41010-I/SN MCP41010-I/SN MCP41010T-I/SN MCP42100T-I/SL MCP42100T-I/SL MCP42100T-I/SL MCP42100T-I/SN MCP421